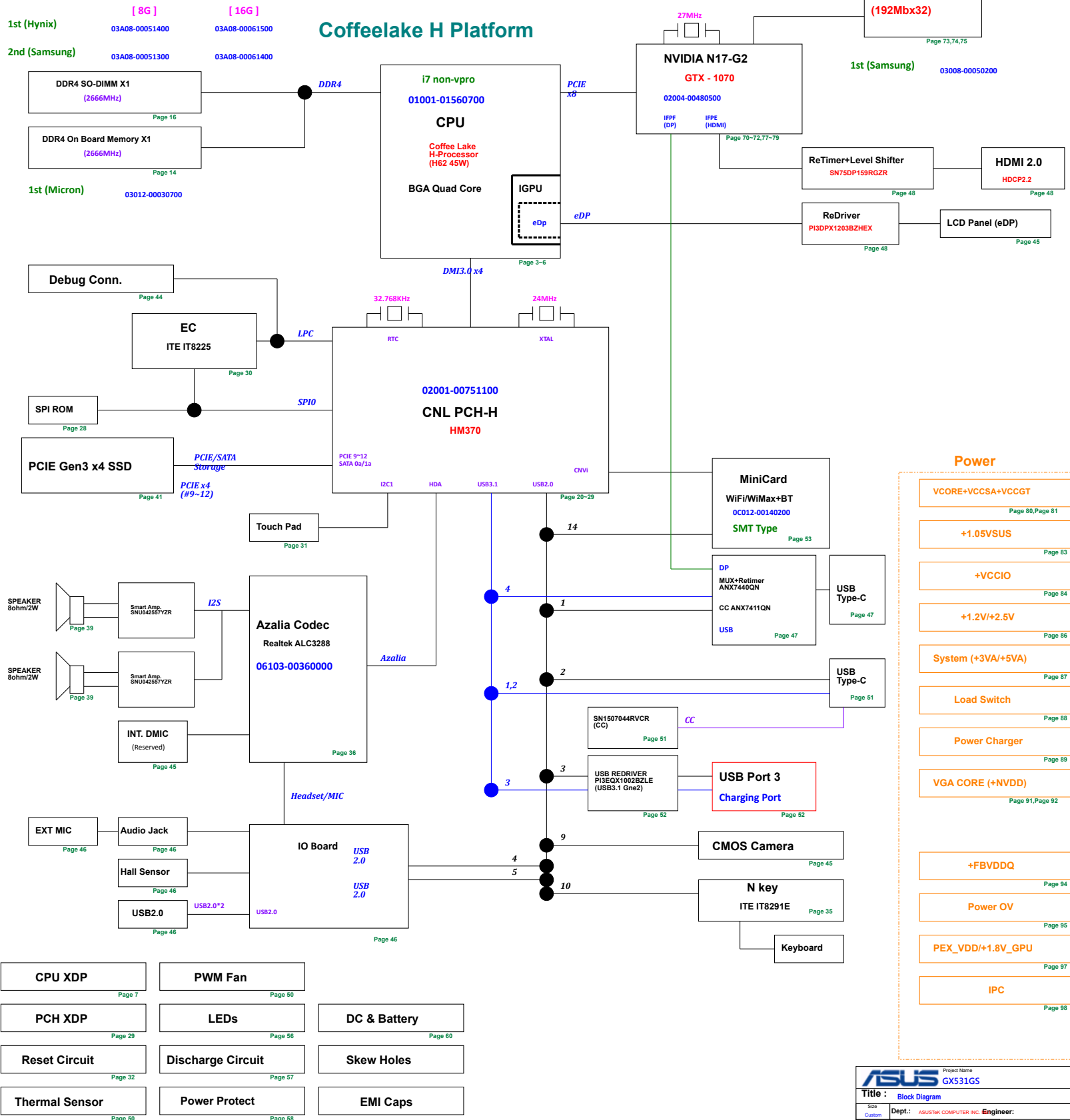


01. Block Diagram
02. System Setting
03. CPU_DMT/PEG/eDP/DDI
04. CPU_DDR4
05. CPU_GND
06. CPU_CFG/RSVD
07. CPU_XDP
08. CPU_PWR
09. CPU_PWR
10. CPU_POWER_CAP
13. DDR4 TERMINATION
14. DDR4_ON-BOARD_A(1)
16. DIMM_DDR4 SO-DIMM B(0) TOP
18. DIM_CA/DQ Voltage
20. PCH-CPT(1)_IHDA/RTC/JTA
21. PCH-CPT(2)_PCIE/LSPC/MISC
22. PCH-CPT(3)_CLK/LPC/USB3
23. PCH-CPT(4)_CRT/eDP/DP
24. PCH-CPT(5)_SPI
25. PCH-CPT(6)_GPIO
26. PCH-CPT(7)_POWER/GND
27. PCH-CPT(8)_POWER/GND
28. PCH-SPI ROM/OTH
29. PCH-XDP
30. KBC_IT8995
31. KBC_KB/TP
32. RST_Reset Circuit
35. Mac6N Key_IT8912E&MG84F5
36. AUD-ALC295CG
37. AUD-Headphone
38. USB3.0 port
39. AUD_INT SPK
41. NGFF_SSD
44. DEBUG_LPC
45. CRT_eDP
46. SB_USB2.0 Audio Jack
47. TYPE-C ANX7440/7411
48. HDMI
49. ANT
50. FAN_Thermal Sensor & Fan
51. USB3.1 Type-C+SN1507044
52. USB3.1 Gen2 port
53. NGFF_Type_WLAN&BT
54. LED Board
55. PowerKeyBoard
56. LED & CON
57. DSG_Discharge
58. PRO_Protect
60. DC/BAT IN
67. screw hold
69. OTH_EMI
70. GPU_PCIE I/F
71. GPU_POWER
72. GPU_FRAME BUFFER
73. VRAM-CHANNEL A
74. VRAM-CHANNEL B
75. VRAM-CHANNEL C
76. VRAM-CHANNEL D
77. VRAM
78. GPU_CLOCK/STRAP/GPIO
79. GPU_LVDS/HDMI/Edp/DP/CRT
80. FW_KABYLAK (1)
81. FW_KABYLAK (2)
83. FW_+1.05VSUS
84. FW_+1.8VSUS
86. FW_+1.2V/+VTT/2.5V
87. FW_+3VADSW/+5VSUS
88. FW_LOAD Switch
89. FW_CHARGER
90. FW_PROTECTION
91. FW_+NVVDD (1)
92. FW_+NVVDD (2)
93. FW_+NVVDDS
94. FW_+FBVDDQ
95. FW_OV
96. FW_+12VS_FAN=>Buck
98. FW_IPC
99. FW_FLOW CHART
100. Power On Timing--AC mode
101. Power On Timing--DC mode
102. History

GM531GX Block Diagram



	Default	Use As	Signal Name	EXT RUPD	Power
0000	A11	000	000_100		
0001	00	000	000_100A	010 100 (R)	+100A 00
0002	00	000	000_V100_100A9	010 100 (R)	+100A 00
0003	A11	000	000_1000		
0004	A11	000	000_1000A		
0005	A11	000	000_1000_000		
0006	A11	000	000_1000_000A		
0007	0	000	000_1000A		
	Default	Use As	Signal Name	EXT RUPD	Power
0000	A11	001	001_100_100A	010 100A	+100A
0001	0	001	001_100_000	010 100A	+100A
0002	00	001	001_100_100A		
0003	A11	001	001_000_000_000A	010 100A	+100A
0004	0	001	001_100_000		
0005	0	001	001_000_000A	010 100A	+100A
0006	00	001	001_100A	010 100A	+100A
	Default	Use As	Signal Name	EXT RUPD	Power
0000	0	001	001_000A	010 100 (R)	+100A 00
0001	A11	0000A	0000_000A	010 470A	+100A 00
0002	A11	0000	0000_000A	010 470A	+100A 00

Output	Input	Unit	Signal Name	EXT RUPID	Power
0001	1	001	001_00101_0000	00_1000	0.0000
0002	0	001	001_00101_0000	00_1000	0.0000
0003	0	001	001_00101_0000	00_1000	0.0000
0004	0	001	001_00101_0000	00_1000	0.0000
0005	0	001	001_00101_0000	00_1000	0.0000
0006	0	001	001_00101_0000	00_1000	0.0000
0007	0	001	001_00101_0000	00_1000	0.0000
0008	0	001	001_00101_0000	00_1000	0.0000
0009	0	001	001_00101_0000	00_1000	0.0000
0010	0	001	001_00101_0000	00_1000	0.0000
0011	0	001	001_00101_0000	00_1000	0.0000
0012	0	001	001_00101_0000	00_1000	0.0000
0013	0	001	001_00101_0000	00_1000	0.0000
0014	0	001	001_00101_0000	00_1000	0.0000
0015	0	001	001_00101_0000	00_1000	0.0000
0016	0	001	001_00101_0000	00_1000	0.0000
0017	0	001	001_00101_0000	00_1000	0.0000
0018	0	001	001_00101_0000	00_1000	0.0000
0019	0	001	001_00101_0000	00_1000	0.0000
0020	0	001	001_00101_0000	00_1000	0.0000
0021	0	001	001_00101_0000	00_1000	0.0000
0022	0	001	001_00101_0000	00_1000	0.0000
0023	0	001	001_00101_0000	00_1000	0.0000
0024	0	001	001_00101_0000	00_1000	0.0000
0025	0	001	001_00101_0000	00_1000	0.0000
0026	0	001	001_00101_0000	00_1000	0.0000
0027	0	001	001_00101_0000	00_1000	0.0000
0028	0	001	001_00101_0000	00_1000	0.0000
0029	0	001	001_00101_0000	00_1000	0.0000
0030	0	001	001_00101_0000	00_1000	0.0000
0031	0	001	001_00101_0000	00_1000	0.0000
0032	0	001	001_00101_0000	00_1000	0.0000
0033	0	001	001_00101_0000	00_1000	0.0000
0034	0	001	001_00101_0000	00_1000	0.0000
0035	0	001	001_00101_0000	00_1000	0.0000
0036	0	001	001_00101_0000	00_1000	0.0000
0037	0	001	001_00101_0000	00_1000	0.0000
0038	0	001	001_00101_0000	00_1000	0.0000
0039	0	001	001_00101_0000	00_1000	0.0000
0040	0	001	001_00101_0000	00_1000	0.0000
0041	0	001	001_00101_0000	00_1000	0.0000
0042	0	001	001_00101_0000	00_1000	0.0000
0043	0	001	001_00101_0000	00_1000	0.0000
0044	0	001	001_00101_0000	00_1000	0.0000
0045	0	001	001_00101_0000	00_1000	0.0000
0046	0	001	001_00101_0000	00_1000	0.0000
0047	0	001	001_00101_0000	00_1000	0.0000
0048	0	001	001_00101_0000	00_1000	0.0000
0049	0	001	001_00101_0000	00_1000	0.0000
0050	0	001	001_00101_0000	00_1000	0.0000
0051	0	001	001_00101_0000	00_1000	0.0000
0052	0	001	001_00101_0000	00_1000	0.0000
0053	0	001	001_00101_0000	00_1000	0.0000
0054	0	001	001_00101_0000	00_1000	0.0000
0055	0	001	001_00101_0000	00_1000	0.0000
0056	0	001	001_00101_0000	00_1000	0.0000
0057	0	001	001_00101_0000	00_1000	0.0000

[illegible]

Device	IO	GPIO	Function	IO	IO#
0001	0	GPIO	TPIC6B015_0C		IO 100
0002	0	GPIO	TPIC6B015_0C		IO 100
0003	0	GPIO	JM1_A15VDDIO		IO 100
0004	0	GPIO	LM2445_0C		IO 100
Device	Default	Use As	Signal Name	EXT RUPD	Power
0010	1	GPIO	HW_VLL_0100		
0011	1	GPIO	HW_VLL_0100		
0012	1	GPIO	ALL_0100VDDIO	IO 100	VDDIO
0013	1	GPIO	0100VDDIO	IO 100V	VDDIO
0014	1	GPIO	0100_VDDIO	IO 100V	VDDIO, VDD
0015	1	GPIO	0100VDDIO		
0016	1	GPIO	0100VDDIO		
0017	A15	A0	A15_A0A_VDDIO		VDDIOA0
0018	A15	A0	HW_VLL_0100	IO 100V + IO 101V	VDDIOA0
Device	Default	Use As	Signal Name	EXT RUPD	Power
0020	0	GPIO	0100_VDDIOA0		
0021	0	GPIO	0100VDDIO	IO 100V	VDDIO, A0
0022	A15	DA	0100VDDIO		
0023	0	GPIO	0100VDDIO + 0100VDDIO_A0		
0024	A15	DA	0100VDDIO		
0025	0	GPIO	0100VDDIO		
0026	0	GPIO	0100VDDIO	IO 100V	VDDIO, A0
0027	0	GPIO	0100VDDIO_A0		

	Default	Use An	Signal Name	EXT PUPB	Power
0000	L0D1_F000		L0D_A00_0_L0DPC_A00		
0001	L0D1_F001		L0D_A00_0_L0DPC_A01		
0002	L0D1_F002		L0D_A00_0_L0DPC_A02		
0003	L0D1_F003		L0D_A00_0_L0DPC_A03		
0004	L0D1_F004		TOP_H0DPC1_P00		
0005	L0D1_F005		TOP_H0DPC1_P01		
0006	L0D1_F006		TOP_H0DPC1_P02		
0007	L0D1_F007		TOP_H0DPC1_P03		
0008	L0D1_F008		TOP_H0DPC1_P04		
0009	L0D1_F009		TOP_H0DPC1_P05		
0010	L0D1_F010		TOP_H0DPC1_P06		
0011	L0D1_F011		TOP_H0DPC1_P07		
0012	L0D1_F012		TOP_H0DPC1_P08		
0013	L0D1_F013		TOP_H0DPC1_P09		
0014	L0D1_F014		TOP_H0DPC1_P10		
0015	L0D1_F015		TOP_H0DPC1_P11		
0016	L0D1_F016		TOP_H0DPC1_P12		
0017	L0D1_F017		TOP_H0DPC1_P13		
0018	L0D1_F018		TOP_H0DPC1_P14		
0019	L0D1_F019		TOP_H0DPC1_P15		
0020	L0D1_F020		TOP_H0DPC1_P16		
0021	L0D1_F021		TOP_H0DPC1_P17		
0022	L0D1_F022		TOP_H0DPC1_P18		
0023	L0D1_F023		TOP_H0DPC1_P19		
0024	L0D1_F024		TOP_H0DPC1_P20		
0025	L0D1_F025		TOP_H0DPC1_P21		
0026	L0D1_F026		TOP_H0DPC1_P22		
0027	L0D1_F027		TOP_H0DPC1_P23		
0028	L0D1_F028		TOP_H0DPC1_P24		
0029	L0D1_F029		TOP_H0DPC1_P25		
0030	L0D1_F030		TOP_H0DPC1_P26		
0031	L0D1_F031		TOP_H0DPC1_P27		
0032	L0D1_F032		TOP_H0DPC1_P28		
0033	L0D1_F033		TOP_H0DPC1_P29		
0034	L0D1_F034		TOP_H0DPC1_P30		
0035	L0D1_F035		TOP_H0DPC1_P31		
0036	L0D1_F036		TOP_H0DPC1_P32		
0037	L0D1_F037		TOP_H0DPC1_P33		
0038	L0D1_F038		TOP_H0DPC1_P34		
0039	L0D1_F039		TOP_H0DPC1_P35		
0040	L0D1_F040		TOP_H0DPC1_P36		
0041	L0D1_F041		TOP_H0DPC1_P37		
0042	L0D1_F042		TOP_H0DPC1_P38		
0043	L0D1_F043		TOP_H0DPC1_P39		
0044	L0D1_F044		TOP_H0DPC1_P40		
0045	L0D1_F045		TOP_H0DPC1_P41		
0046	L0D1_F046		TOP_H0DPC1_P42		
0047	L0D1_F047		TOP_H0DPC1_P43		
0048	L0D1_F048		TOP_H0DPC1_P44		
0049	L0D1_F049		TOP_H0DPC1_P45		
0050	L0D1_F050		TOP_H0DPC1_P46		
0051	L0D1_F051		TOP_H0DPC1_P47		
0052	L0D1_F052		TOP_H0DPC1_P48		
0053	L0D1_F053		TOP_H0DPC1_P49		
0054	L0D1_F054		TOP_H0DPC1_P50		
0055	L0D1_F055		TOP_H0DPC1_P51		
0056	L0D1_F056		TOP_H0DPC1_P52		
0057	L0D1_F057		TOP_H0DPC1_P53		
0058	L0D1_F058		TOP_H0DPC1_P54		
0059	L0D1_F059		TOP_H0DPC1_P55		
0060	L0D1_F060		TOP_H0DPC1_P56		
0061	L0D1_F061		TOP_H0DPC1_P57		
0062	L0D1_F062		TOP_H0DPC1_P58		
0063	L0D1_F063		TOP_H0DPC1_P59		
0064	L0D1_F064		TOP_H0DPC1_P60		
0065	L0D1_F065		TOP_H0DPC1_P61		
0066	L0D1_F066		TOP_H0DPC1_P62		
0067	L0D1_F067		TOP_H0DPC1_P63		
0068	L0D1_F068		TOP_H0DPC1_P64		
0069	L0D1_F069		TOP_H0DPC1_P65		
0070	L0D1_F070		TOP_H0DPC1_P66		
0071	L0D1_F071		TOP_H0DPC1_P67		
0072	L0D1_F072		TOP_H0DPC1_P68		
0073	L0D1_F073		TOP_H0DPC1_P69		
0074	L0D1_F074		TOP_H0DPC1_P70		
0075	L0D1_F075		TOP_H0DPC1_P71</		

12	POIC #6	QIC#	X,2	NA	12	POIC #6	
13	POIC #7		X,2		13	POIC #7	
14	POIC #8		X,2		14	POIC #8	
15	POIC #9	SATA #0	QIC#		15	POIC #9	
16	POIC #10	SATA #1			16	POIC #10	
17	POIC #11		X,2		total TRST POIC Storage Device #1	17	POIC #11
18	POIC #12	QIC#	X,2			18	POIC #12
19	POIC #13	SATA #0	QIC#			19	POIC #13
20	POIC #14	SATA #1				20	POIC #14
21	POIC #15	SATA #2	X,2		total TRST POIC Storage Device #2	21	POIC #15
22	POIC #16	SATA #3	X,2	22		POIC #16	
23	POIC #17	SATA #4	X,2	total TRST POIC Storage Device #3	23	SATA #4	
24	POIC #18	SATA #5			24	SATA #5	
25	POIC #19	SATA #6			25	POIC #19	
26	POIC #20	SATA #7	X,2		26	POIC #20	

N501VW Setting

SM_BUS ADDRESS :

PCB Number	SM-Bus Number	SM-Bus Address
PCB Model / Assembly Code	Auto	
SD-CORR BUS		

[illegible]

05	USBDMS2	USB2.0 MBP (Charger)	
06	USBDMS1 / PCKMS1	USB2.0 P-Port	
07	USBDMS3 / PCKMS2	USB2.0 P-Port	
08	USBDMS4	USB2.0 P-Port	
09	USBDMS5		
0A	USBDMS6		
0B	USBDMS7 / PCKMS3	CardReader_USB2000	
0C	USBDMS8 / PCKMS4		MS2
0D	PCKMS2	WLAN	MS1
0E	PCKMS3 / GMS		
0F	PCKMS4 / GMS	Thunderbolt	MS3
10	PCKMS5		
11	PCKMS6		
12	PCKMS7		
13	PCKMS8		
14	PCKMS9		
15	PCKMS10 / USBDMS7 / GMS	SATA1.5 SSD port0	
16	PCKMS11 / USBDMS8	PCK1.5 SSD	MS4
17	PCKMS12		
18	PCKMS13 / GMS		
19	PCKMS14 / USBDMS9 / GMS		

23	PC/SP415 / GARDAS		
23	PC/SP415 / GARDAS		
23	PC/SP415 / GARDAS		
24			
25			
26			

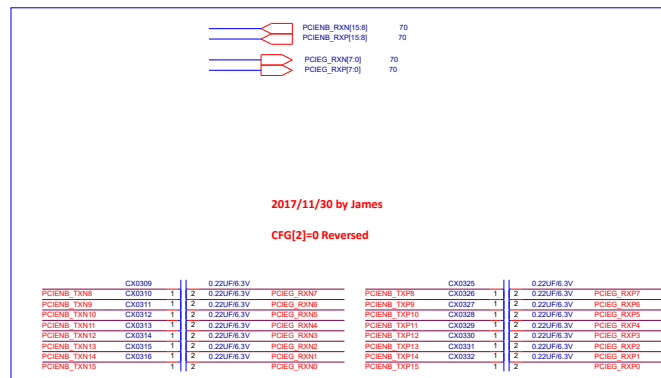
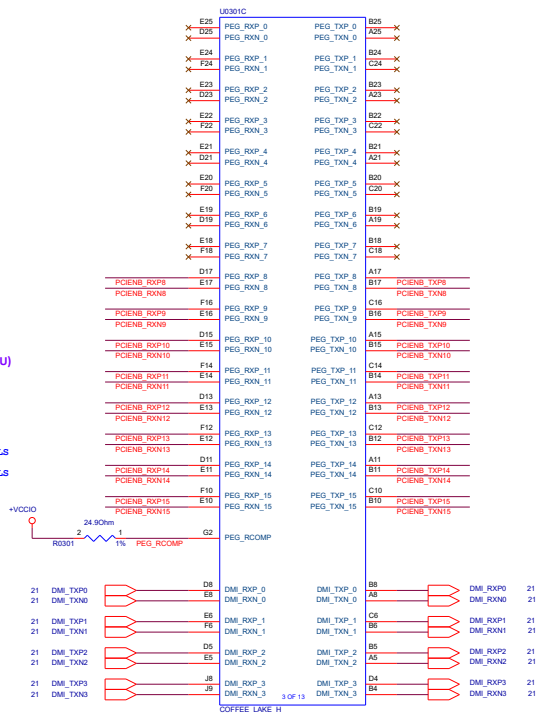
PCH H170 HSIO					SKL PCH H170 HSIO				
SSIC #1					1) USB3 #1 (OTG)				
SSIC #2					2) USB3 #2		SSIC #1		
					3) USB3 #3		SSIC #2		
					4) USB3 #4				
					5) USB #5				
					6) USB #6				
					7) USB #7				
					8) USB #7	PCIe #1			
					9) PCIe #3	PCIe #2	x,2		
					10) PCIe #4			x,4	NA
QbE	x,2	NA			11) PCIe #5	QbE			
QbE					12) PCIe #6	QbE			
	x,4				13) PCIe #7		x,2		
		NA			14) PCIe #8			x,4	NA
					15) PCIe #7				
					16) PCIe #9		QbE		
QbE					17) PCIe #9	SATA #0		x,2	Intel I/O PCIe Storage Device #1
QbE	x,4				18) PCIe #10	SATA #1			
QbE					19) PCIe #11			x,4	Intel I/O PCIe Storage Device #2
QbE					20) PCIe #12	QbE			
QbE					21) PCIe #13	SATA #0	QbE		
QbE	x,4				22) PCIe #14	SATA #1			
QbE					23) PCIe #15	SATA #2		x,4	Intel I/O PCIe Storage Device #3
QbE					24) PCIe #16	SATA #3			
					25)				
					26)				
					27)				
					28)				
					29)				
					30)				
					31)				
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					60)				
					61)				
					62)				

Function
USB 2.0 MB Port(Charger)
USB 2.0 MB Port2
USB 2.0 MB Port3
Camera
USB 2.0 MB Port4
Card Reader
IR key
BT

AS E

dGPU
(AC-CAP Place on dGPU)

Trace length < 400 MILS
Trace width = 12 MILS
Trace spacing = 15 MILS



Display

2017/11/16 Add HDMI/TBT/eDP interface for MS-Hybrid by James

31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. $\sim 2K\Omega$), PROC_AUDIO_SDO can be left unconnected.

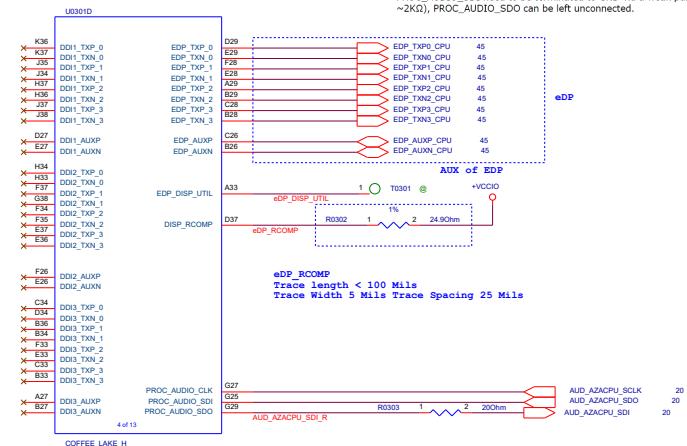


Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	Physical Lanes															
				0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Off	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

1. Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
2. In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.

For example:

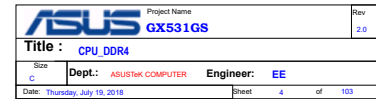
- a. When using $1 \times 8 + 2 \times 4$, the 8 lane device must use lanes 0:7.
- b. When using $1 \times 4 + 1 \times 2$, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
- c. When using $1 \times 4 + 1 \times 2 + 1 \times 1$, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.

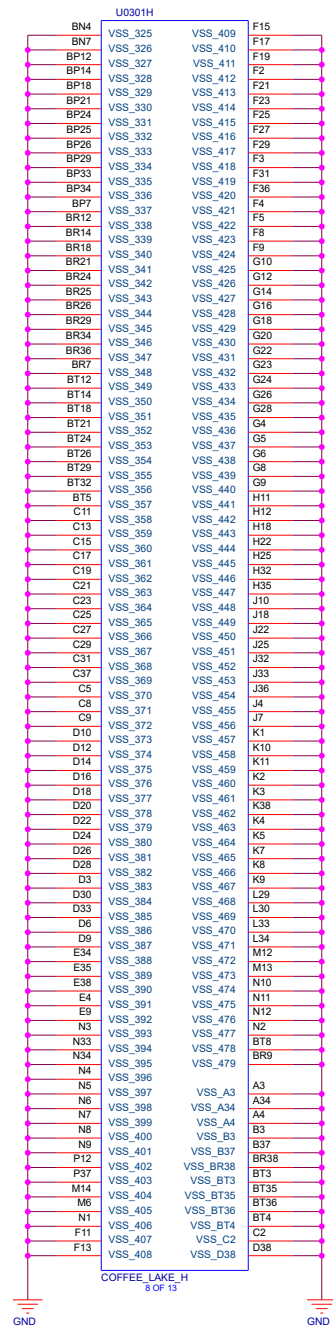
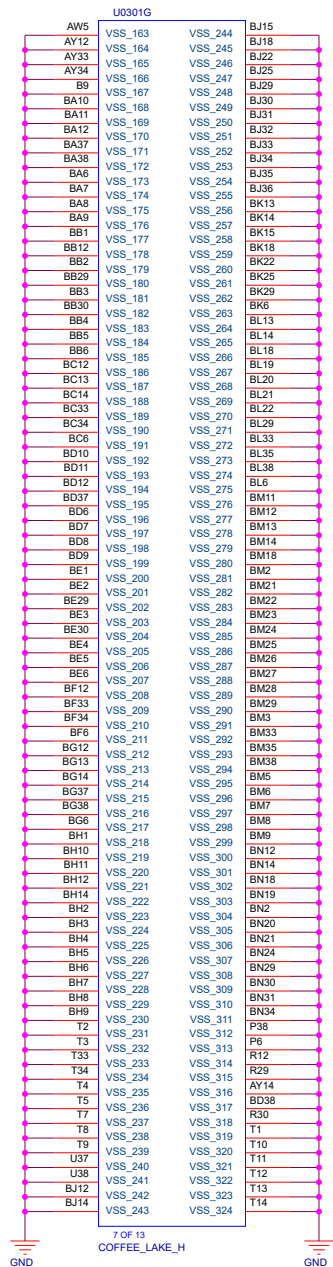
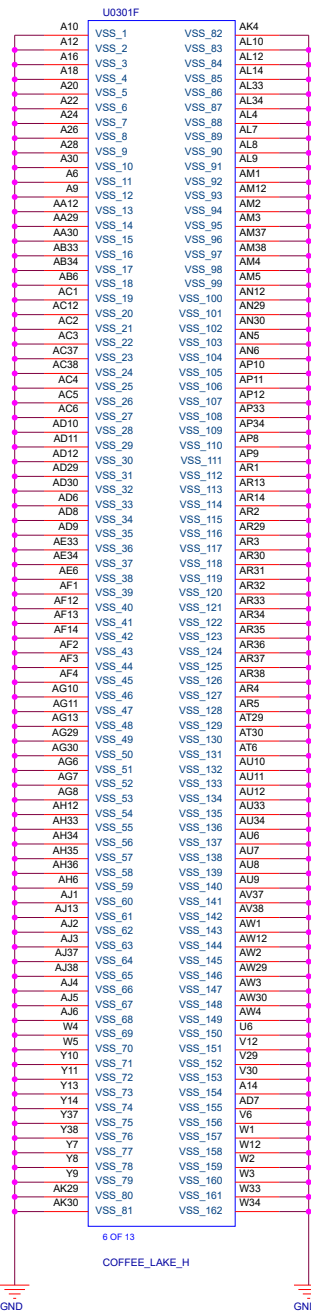
Refer to CFL-H PDG P.363 (Doc.571391)

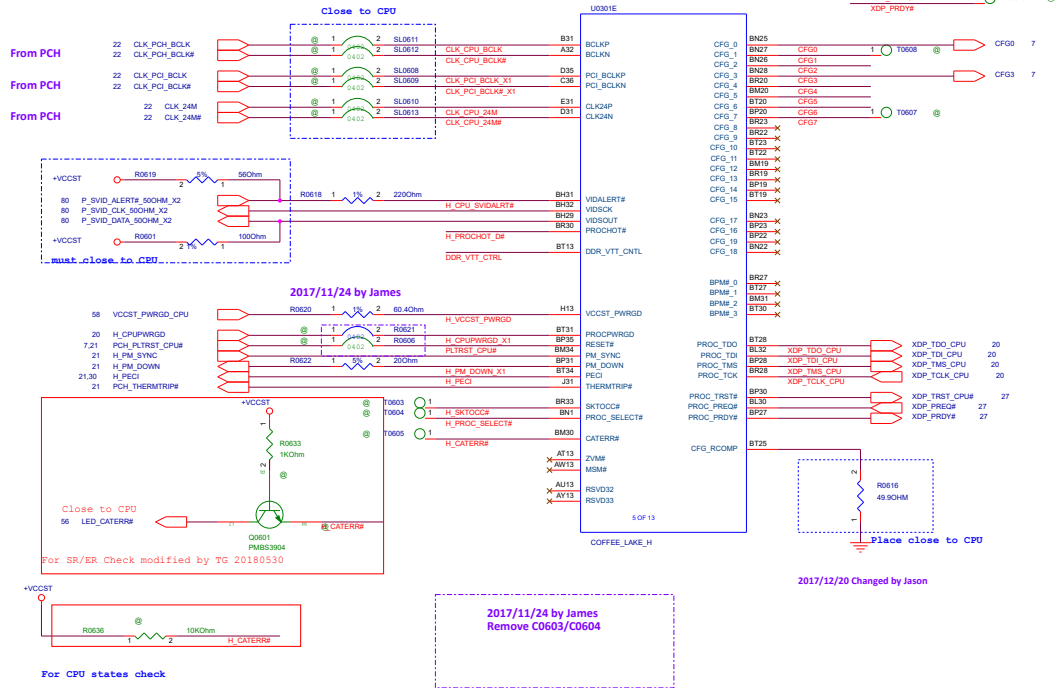
31.1.4 Disabling and Termination Guidelines for the Intel® High Definition Audio Interface

When HDA_SDIN[1:0], DISPA_SDIN interface is not implemented on the platform the signal pin(s) may be left unconnected.

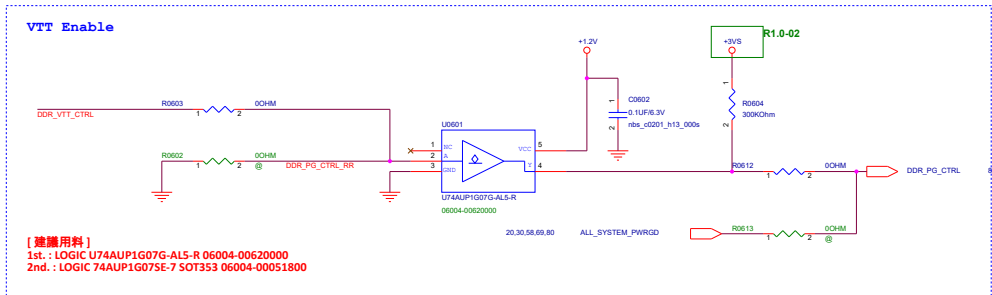
When the Intel® Display Audio interface is not implemented, PROC_AUDIO_CLK and PROC_AUDIO_SDI need to be terminated to GND via a weak pull-down resistor (i.e. $\sim 2K\Omega$), PROC_AUDIO_SDO can be left unconnected.



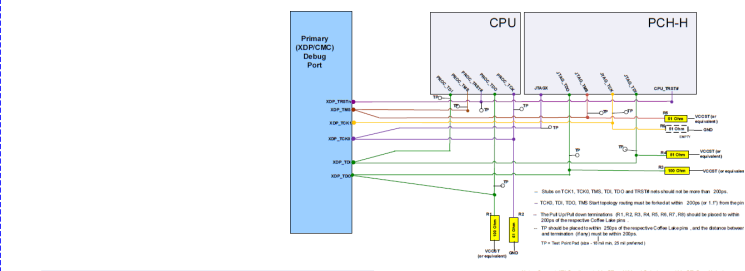
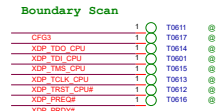
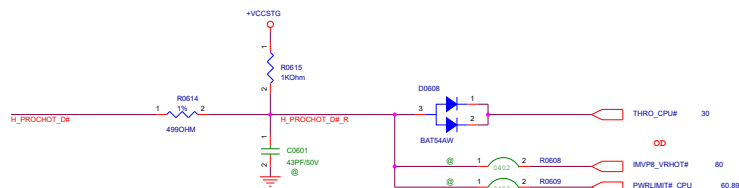




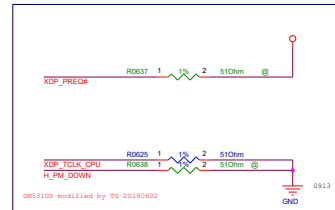
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref: Intel 570805_Coffeelake_EDS_Vol_1_Rev1.5 P.116



CPU SIDEBAND SIGNALS

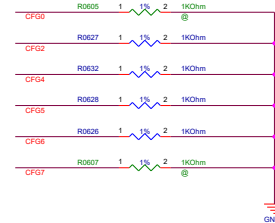


Note: Connect JTAG pull-ups to Vcc5T on U/Y and S designs and Vcc5T-G on H designs.



CFG Straps

2017/11/16 by James
1. Changed R0632 to stuff for eDP enable
2. Changed R0628/R0626 to stuff for PCIEx16



CFG Straps for Processor

ref : Intel 570805_Coffeelake_EDS_Vol_1_Rev1.4 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express® Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express® Bifurcation

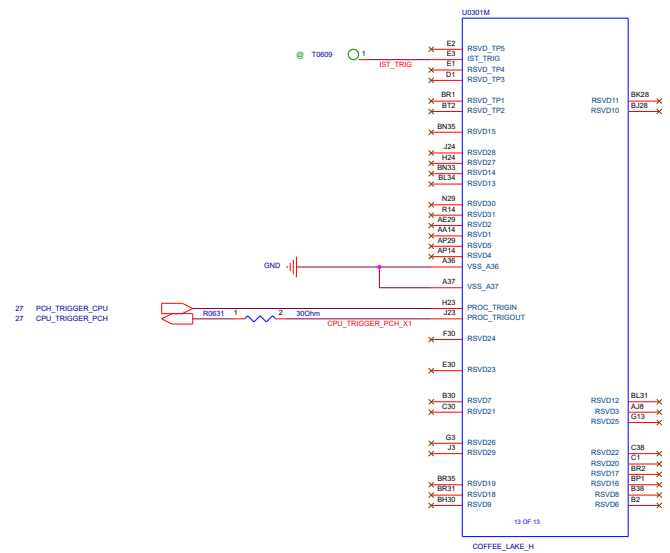
- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

CFG[7] : PEG Training

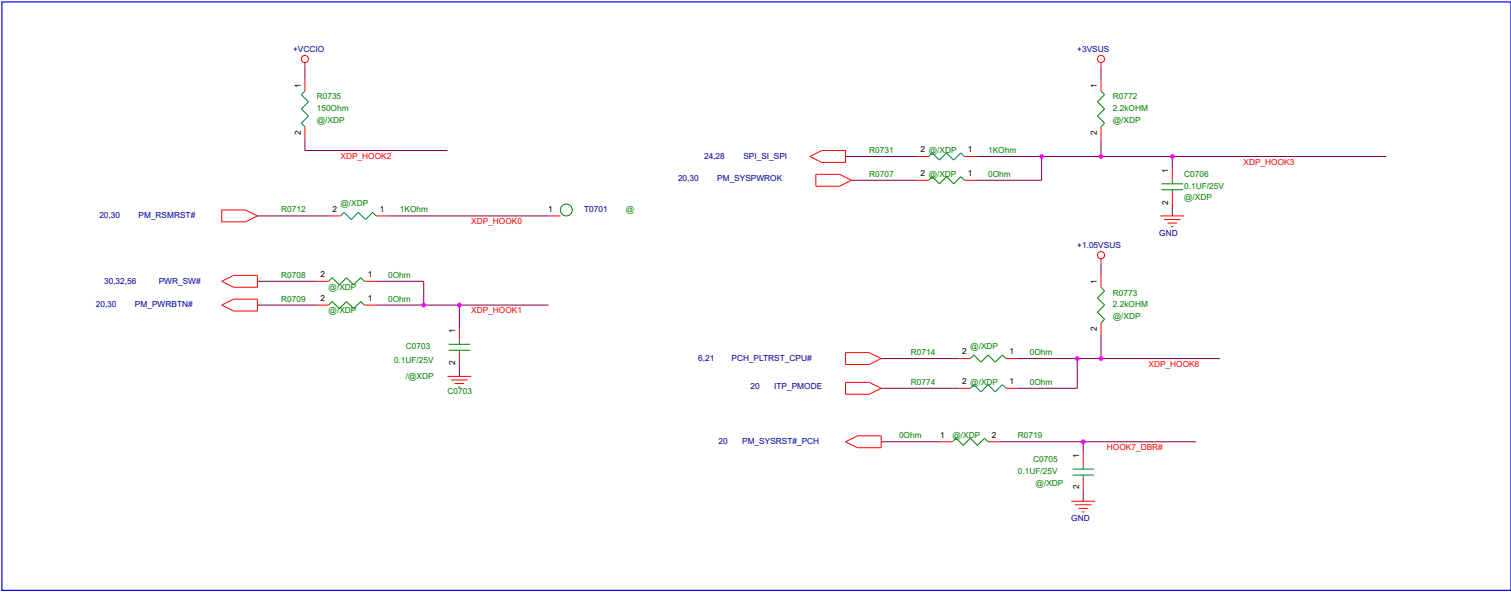
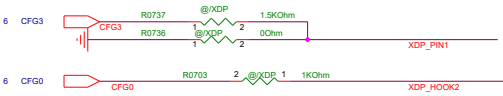
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

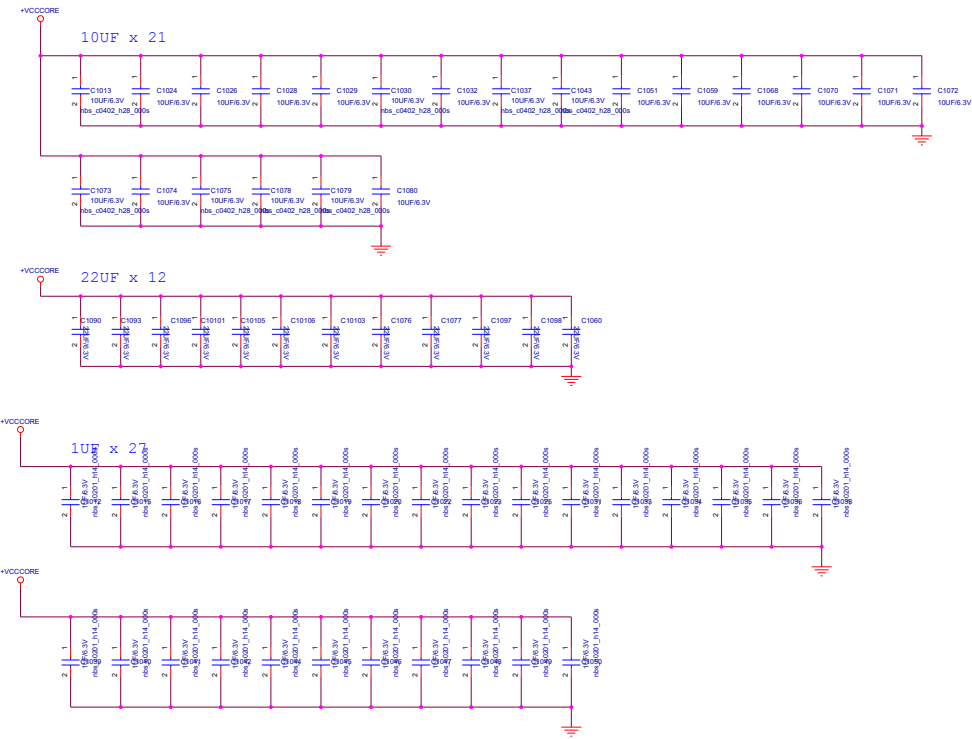
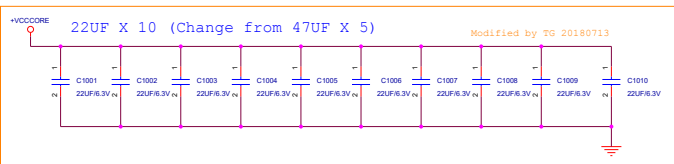
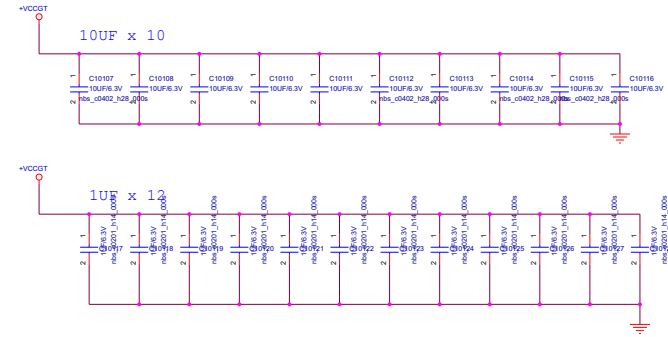
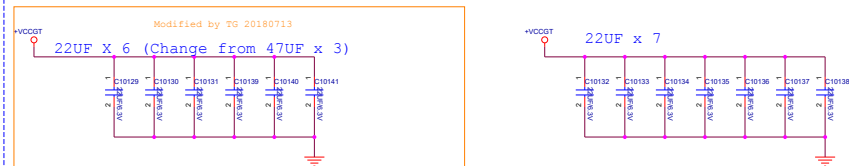
CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes




CPU XDP



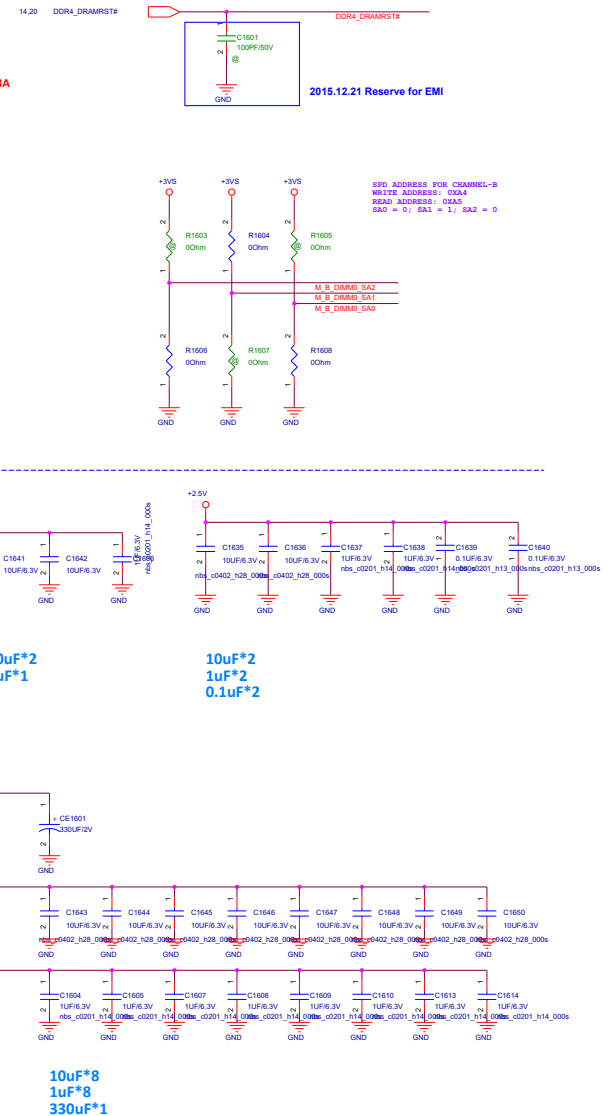
+VCCORE DECAPS Place Back Side (TOP)**+VCCORE near CPU****+VCCGT DECAPS Place Back Side (TOP)****+VCCGT near CPU**

Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805		
		12x 22uF 0603	
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
VccGT	3x 47uF 0805		Place as close to the BGA as possible
	7x 22uF 0603		
		10x 10uF 0402	
		12x 1uF 0201	


		Project Name	Rev
Title :		CB IO CON	2.0
Size	Dept.:		
B	ASUSTek COMPUTER INC. Engineer:		
Date: Thursday, July 10, 2018	Sheet	12	of 103

		Title : DDR4_ON-BOARD_A2	
ASUSTeK COMPUTER INC.		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 15 of 103	

Main Board



DDR4 - 2666MHz (8G)
1st : Hynix - 03A08-00051400
2nd : Samsung - 03A08-00051300
DDR4 - 2666MHz (16G)
1st : Hynix - 03A08-00061400
2nd : Samsung - 03A08-00061500

	Project Name		Rev
	GX531GS		2.0
Title : DIM_DDR4 SO-DIMM B1			
Size	Dept.: ASUSTeK COMPUTER INC. Engineer: EE		
C			
Date: Thursday, July 19, 2018		Sheet	16 of 103


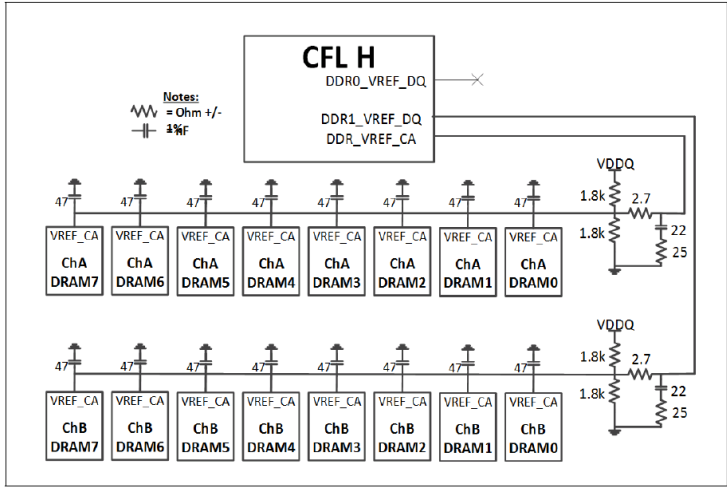
		Title : NB_****	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 17 of 103	

Figure 4-24. CFL-H DDR4 x8 Memory Down V_{REF-CA} Overview



Memory Down Vref

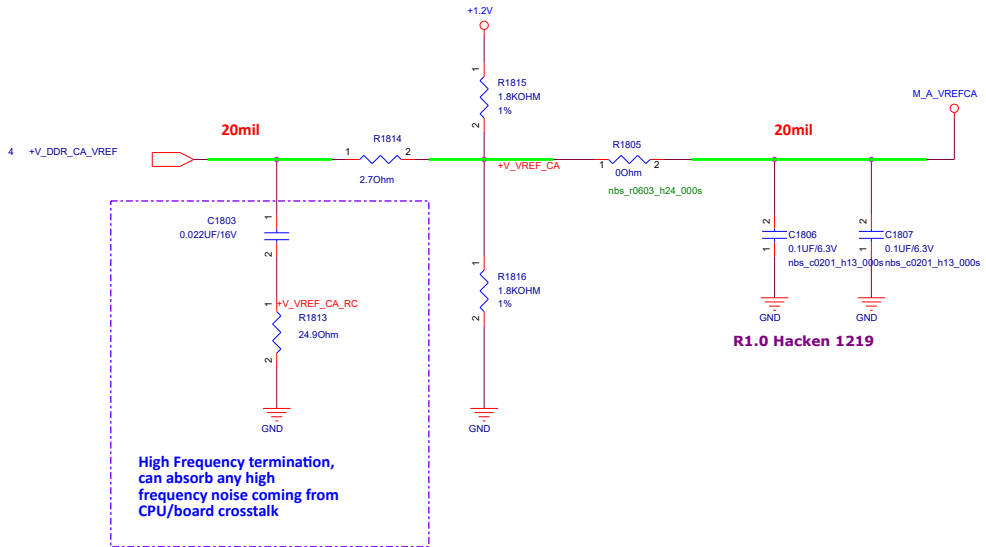
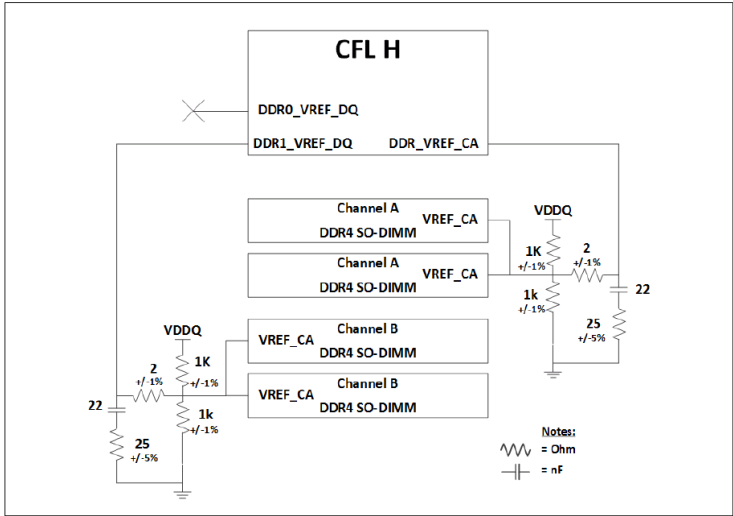
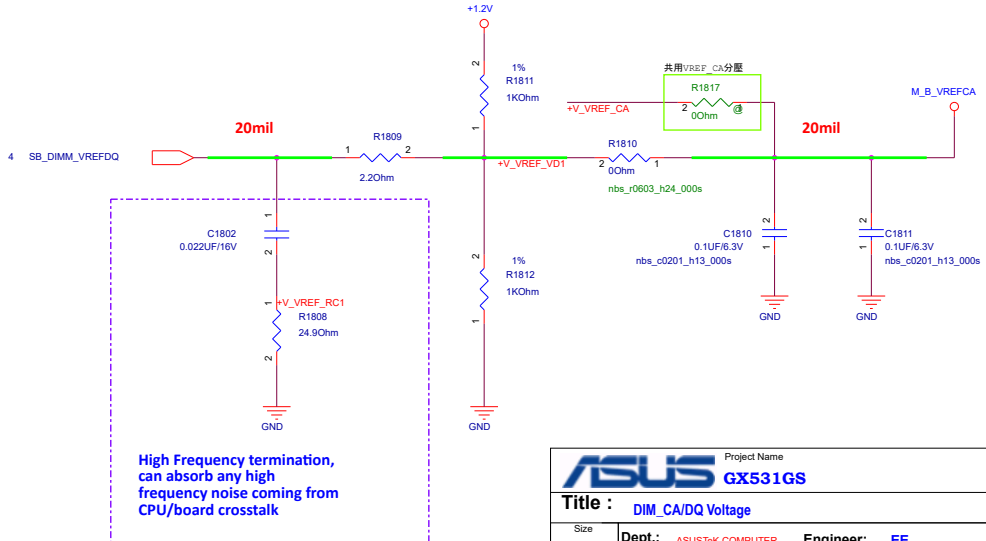



Figure 4-22. CFL-H DDR4 SO-DIMM V_{REF-CA} Overview



SO-DIMM1 Vref



		Title : *****	
ASUSTeK COMPUTER INC. NB3		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 19 of 103	

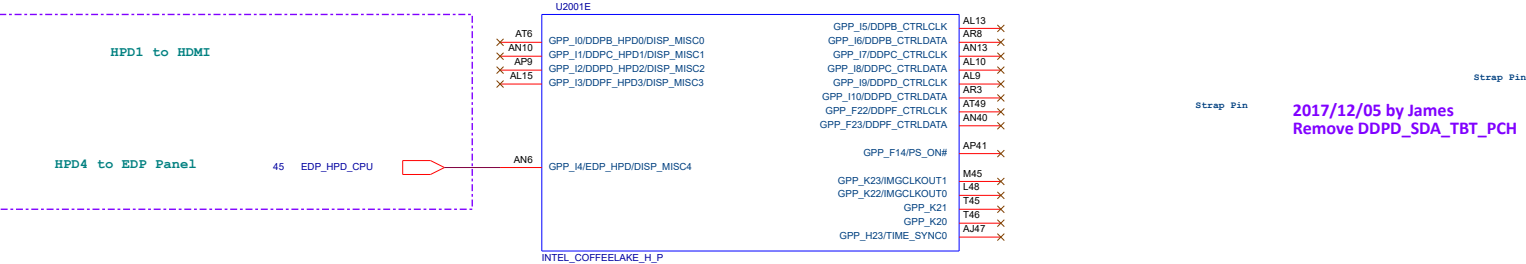
Main Board

- HPD0 to DP
- HPD1 to HDMI
- HPD2 to TBT
- HPD3 to VGA
- HPD4 to EDP Panel

2017/11/16 by James
1. Add DDI3_TBT/HDMI/eDP_HPD for MS-Hybrid design
2. Remove R2301

2017/12/05 by James
Remove DDI3_TBT_PD

2017/12/26 by James
Remove DDI2_HDMI_HPD



DDP Strap Setting Update:
0 = Port is not detected (Default)
1 = Port is detected

2017/12/05 by James
Remove DDPD_SDA_TBT_PCH

DDP Strap Setting Update:
0 = Port is not detected (Default)
1 = Port is detected

GPP_I6 / DDPB_CTRLDATA	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I8 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_I10 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well.
GPP_F23	Display Port F Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port F is not detected. (Default) 1 = Port F is detected. Notes: 1. The internal pull-down is disabled after PCH_PWROK de-asserts. 2. This signal is in the primary well. 3. This strap applies to platforms that support Display Port F only. Refer to the platform's processor documentation for info on Display Port F support.

5.6 Digital Display Interface Disabling and Termination Guidelines

All the digital display ports on the Coffee Lake processor have a strap associated with it. The port strap needs to be set to configure each digital port irrespective of the digital display technology HDMI/DP. The following table lists all the digital display straps and guidelines to enable/disable a respective port on the platform. All the straps are sampled on the rising edge of the PWROK signal.

Table 5-15. DDI Disabling and Termination Guidelines

Port	Strap	How to Enable PortΩ	How to Disable PortΩ
Port 1	DDPB_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 2	DDPC_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect
Port 3	DDPD_CTRLDATA	Pull up to 3.3V with 2.2K ohm ±5% resistor	No Connect

GPIO Voltage Level

Group	Power pin	Power option	Power plane
GPIO_A	VCCPGPA	3.3V	+3VSUS
GPIO_B	VCCPGPBC	3.3V	+3VSUS
GPIO_C	VCCPGPC	3.3V	+3VSUS
GPIO_D	VCCPGPD	1.8V or 3.3V	+1.8VSUS
GPIO_E	VCCPGPEP	3.3V	+3VSUS
GPIO_F	VCCPGPEF	3.3V	+3VSUS
GPIO_G	VCCPGPG	Dynamic voltage to be config GPIO	+3VSUS +1.8VSUS
GPIO_H	VCCPGPHE	3.3V	+3VSUS
GPIO_I	VCCPGPIH_3P3	3.3V Only	+3VSUS
GPIO_J	VCCPGPIH_1P8	1.8V Only	+1.8VSUS
GPIO_K	VCCPGPK	3.3V	+3VSUS
GPIO	VCCDWM_3P3	3.3V Only	+3VA_DWM

Table B-1. Power Descriptions for PCH in CNL-H

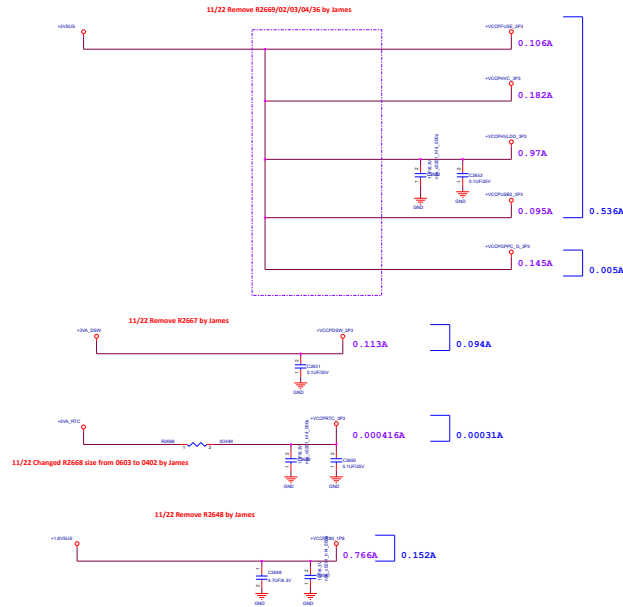
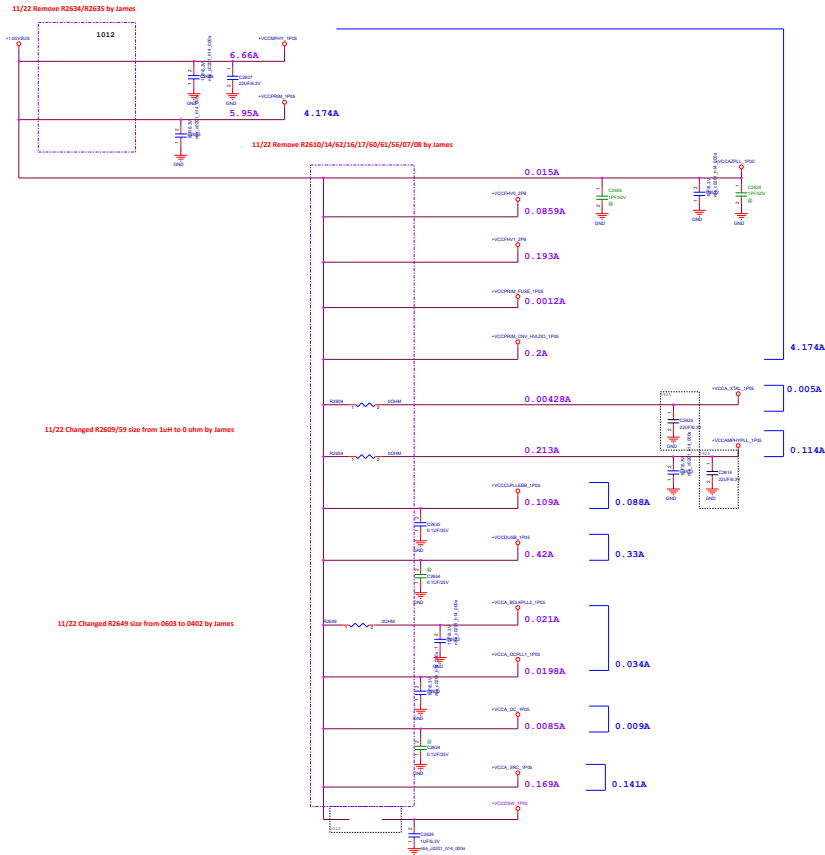
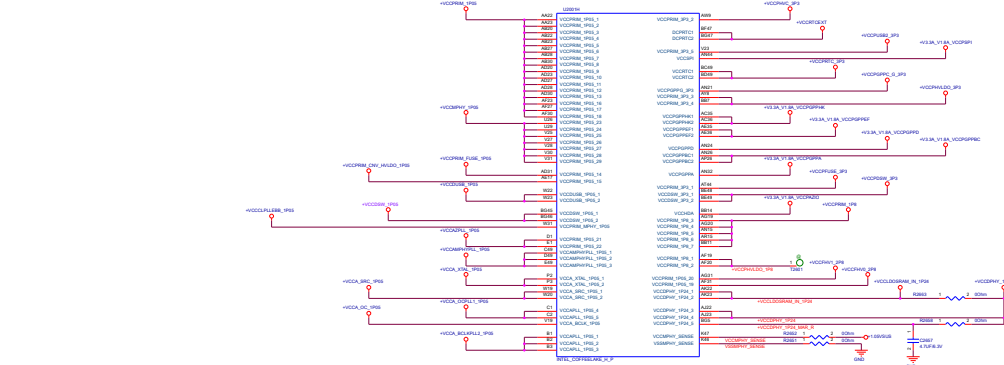
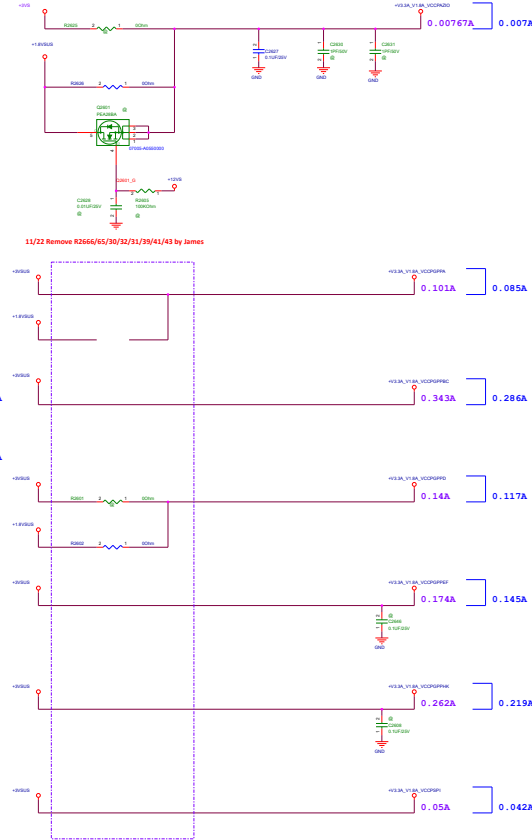
Name	Description
VCCPHVLD0_LP8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPHVLD0_LP8 and to Internal 1.8 V VHM Mode and not to VCCPHVLD0_LP8.
VCCPHVLD0_LP8	AF19
VCCPHVLD0_LP8	AF20

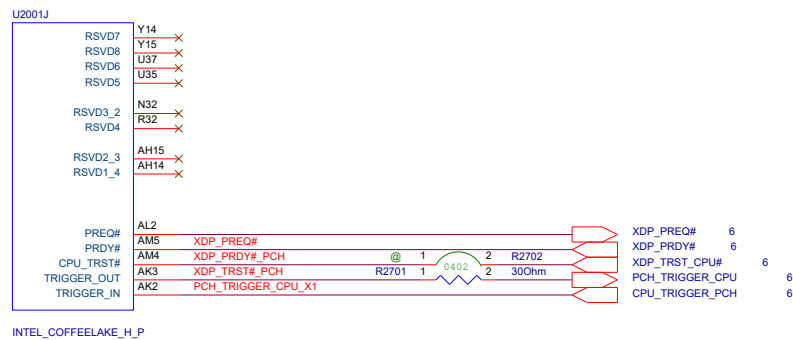
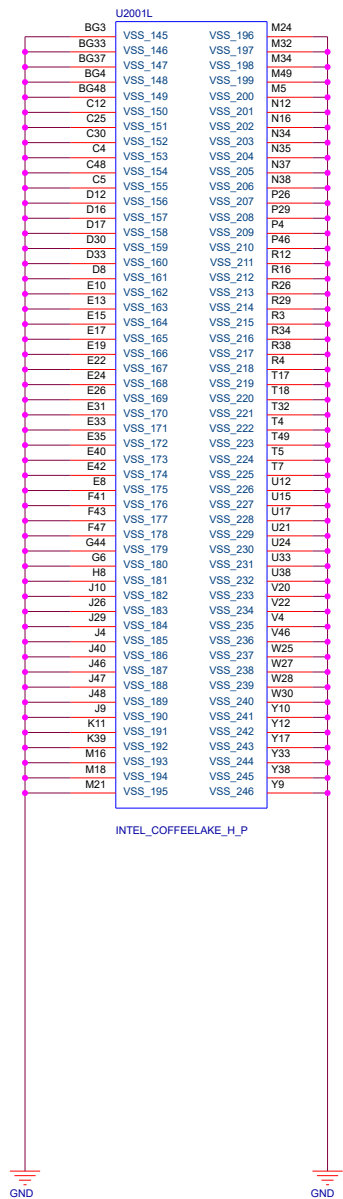
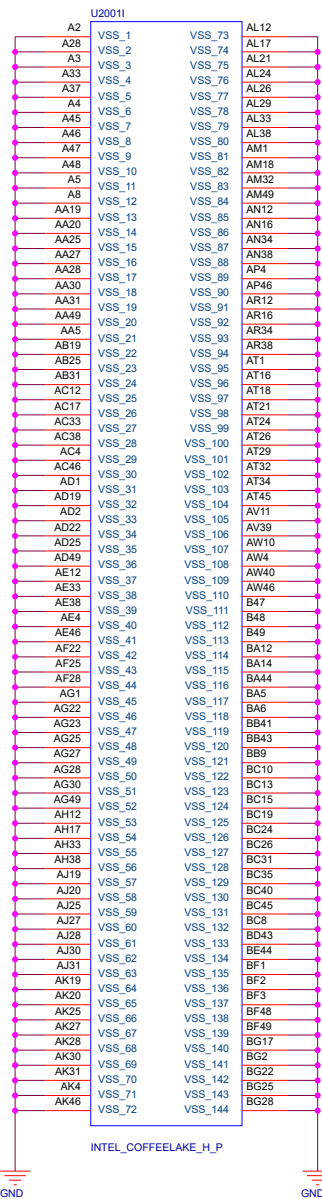
VCCPHY_LP24	1.24V for CNV logic. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Cannon Lake -IYT PEG for implementation details.
-------------	---




SHORT PCH PINS A22, A23, AX22, AX23 TOGETHER IN SURFACE LAYER AND CONNECT BGS TO EDGE CAP WITH LOWEST LOOP INDUCTANCE AS PEG RECOMMENDS.

Purple reference C8B
Blue reference EDS





		Project Name	Rev
		GX531GS	2.0
Title : TEST POINT			
Size B	Dept.: ASUSTeK COMPUTER	Engineer: EE	
Date: Thursday, July 19, 2018	Sheet	29	of 103

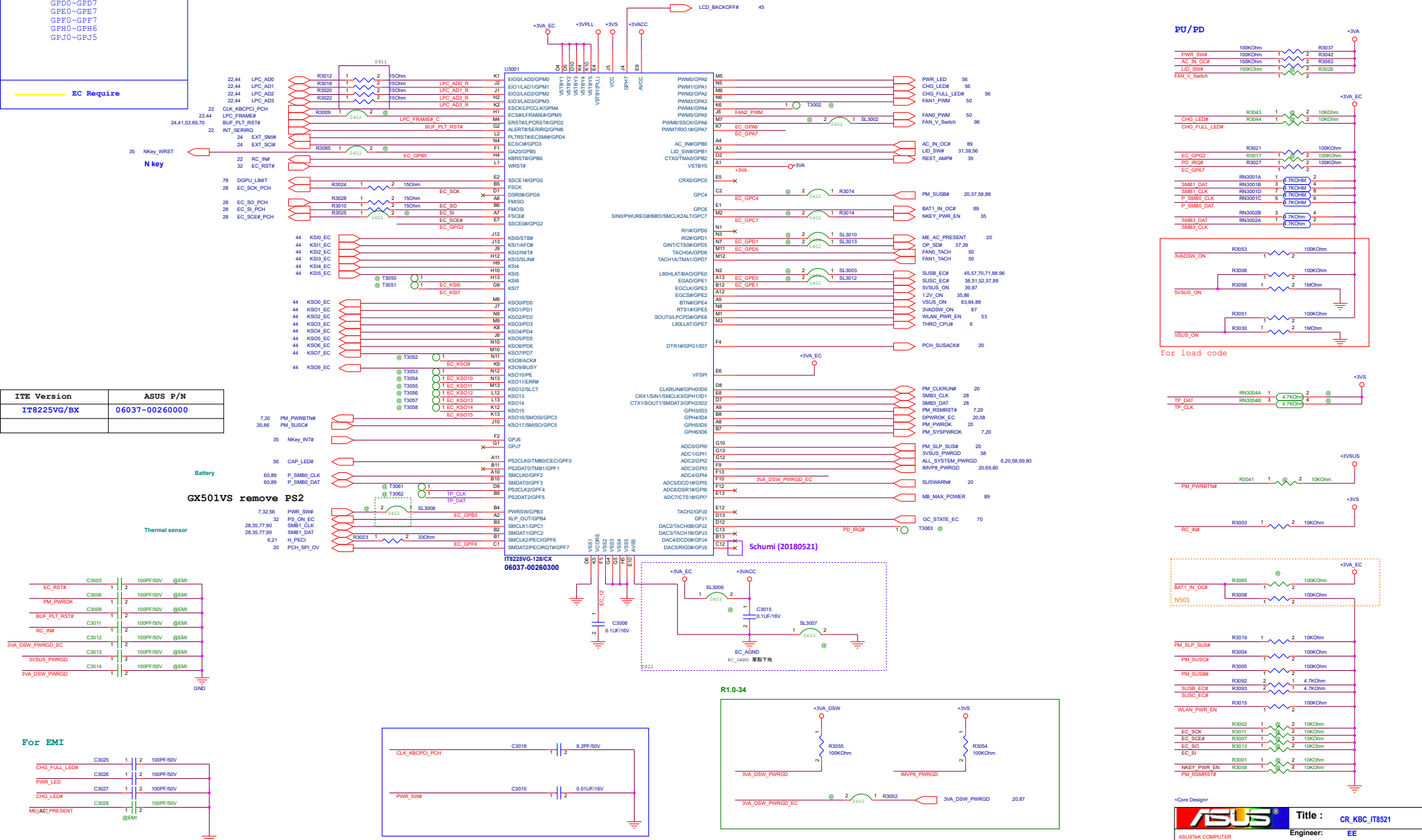
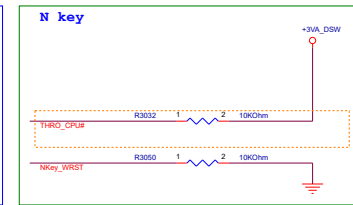
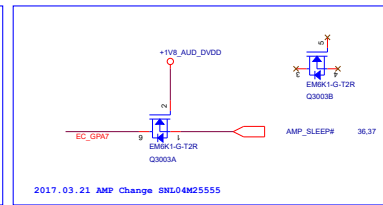
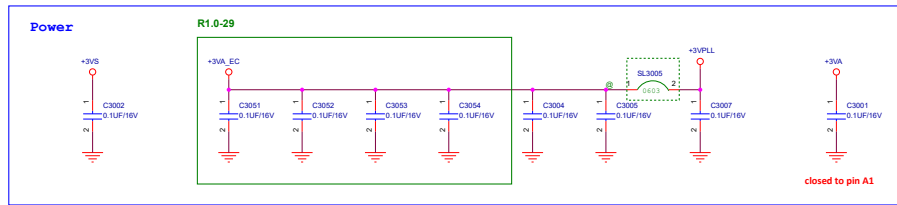
Only 3V Torlence

```
GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 :7]
GPJ[0:7]
```

Can be adjusted to
Open-Drain for port:

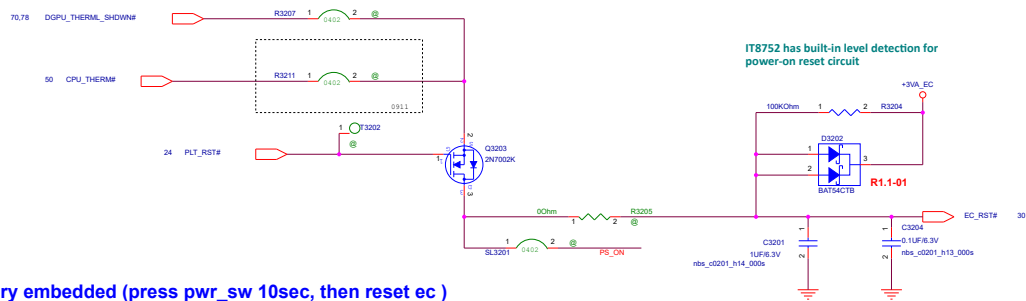
GPA0~GPA3
GPB0~GPB7
GPD0~GPD7
GPE0~GPE7
GPF0~GPF7
GPH0~GPH6
GPJ0~GPJ5

EC Require

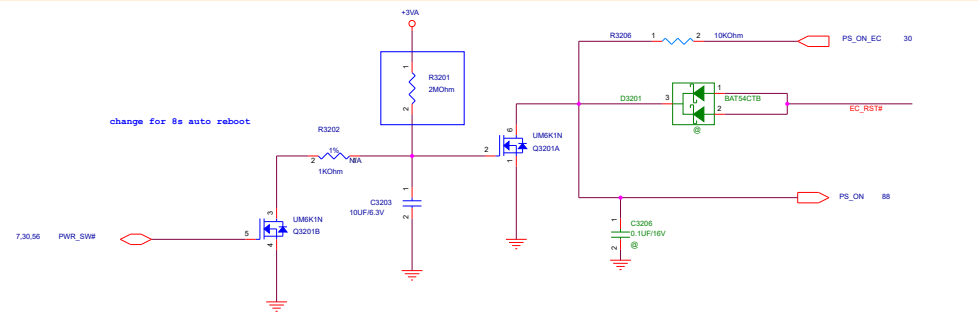


Thermal Policy

Reset Circuit



Battery embedded (press pwr_sw 10sec, then reset ec)





EC power off solution:
 Solution1 Mount R3206, D3201/ Unmount R3216
 Solution2 Mount R3206/R3216/ Unmount D3201- for reserved 0402 footprint

R1. 2-65

<Core Design>

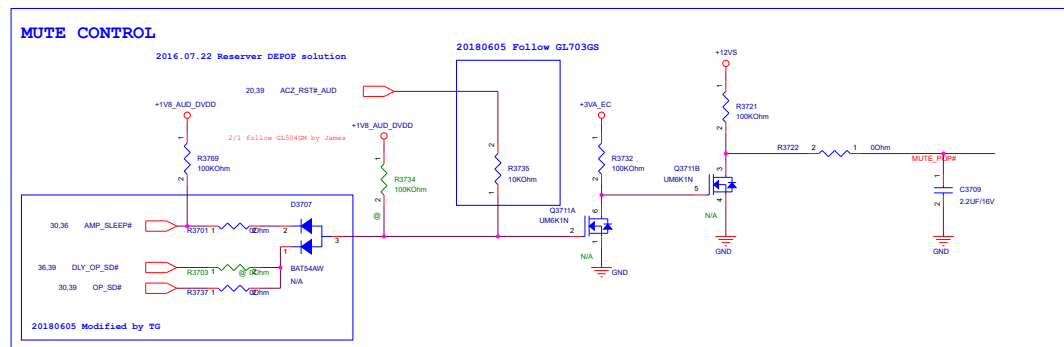
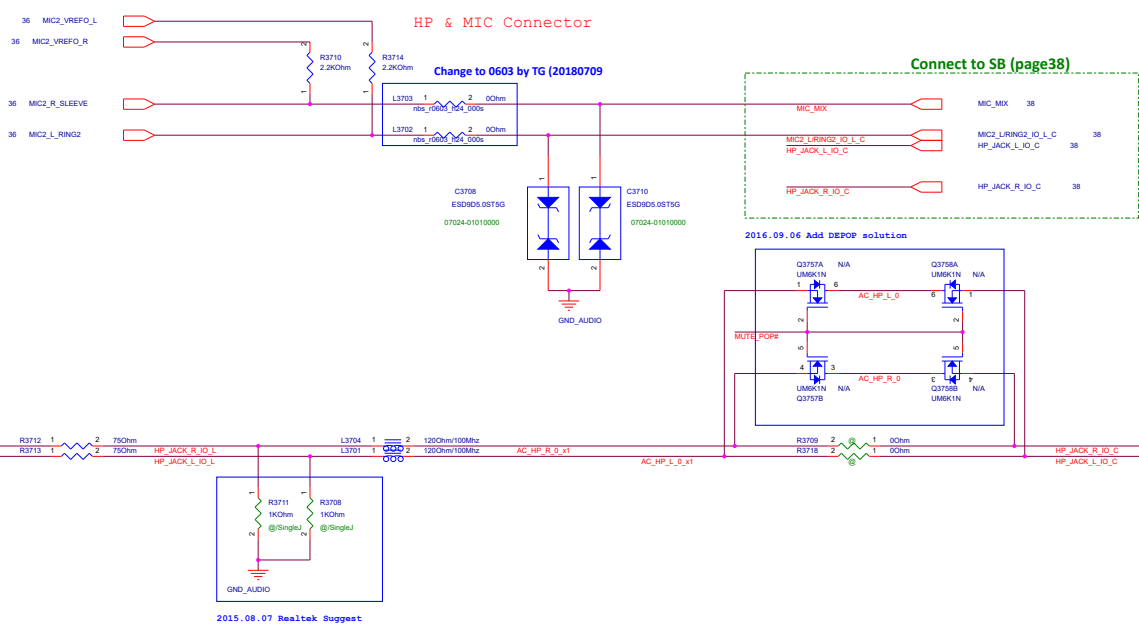
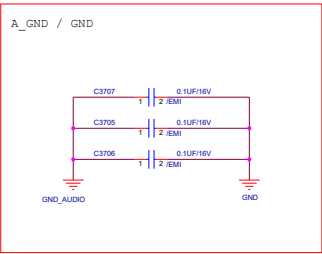
ASUS		Title : RST_Reset Circuit	
ASUSTek COMPUTER		Engineer: EE	
Size	Project Name	Rev	
B	GX531GS	2.0	
Date: Thursday, July 19, 2018	Sheet	32	of 103

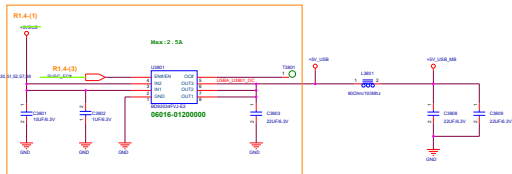
		Project Name	Rev
		GX531GS	2.0
Title : LAN RTL8111GUX-CG			
Size	Dept.: ASUSTeK COMPUTER INC. Rev Engineer:		
A			
Date: Thursday, July 19, 2018	Sheet	33	of 103

		Project Name	Rev
		GX531GS	2.0
Title : LAN RJ45 Conn.			
Size	Dept.: ASUSTeK COMPUTER INC. Rev Engineer:		
A			
Date: Thursday, July 19, 2018	Sheet	34	of 103

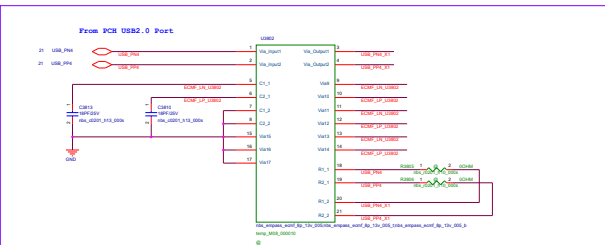
Headphone&MIC

Main Board



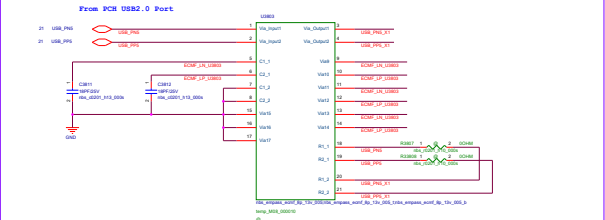


USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



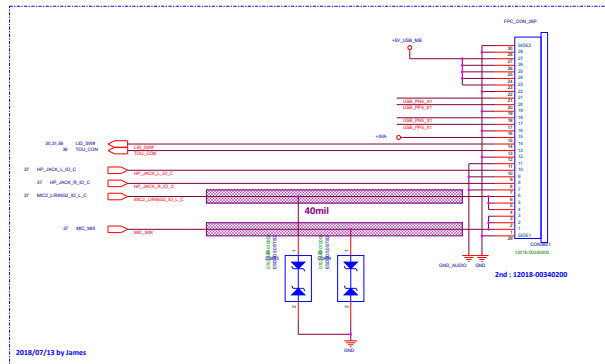
- Note :**
1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
 2. C3809&C3810 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
 3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
 4. Pin13 to Pin16 are floated in regular scheme

R1.5 USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)



- Note :**
1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I
Please check your project must matching the thickness , DF and DK value of PCB every layer
 2. C3811&C3812 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5%
 3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground
 4. Pin13 to Pin16 are floated in regular scheme


Connect to Sub Board (Page46)



2018/07/13 by James

temp_M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

temp M08_000010層名順序是：TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

		Title : MiniCard_SSD	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 40 of 103	

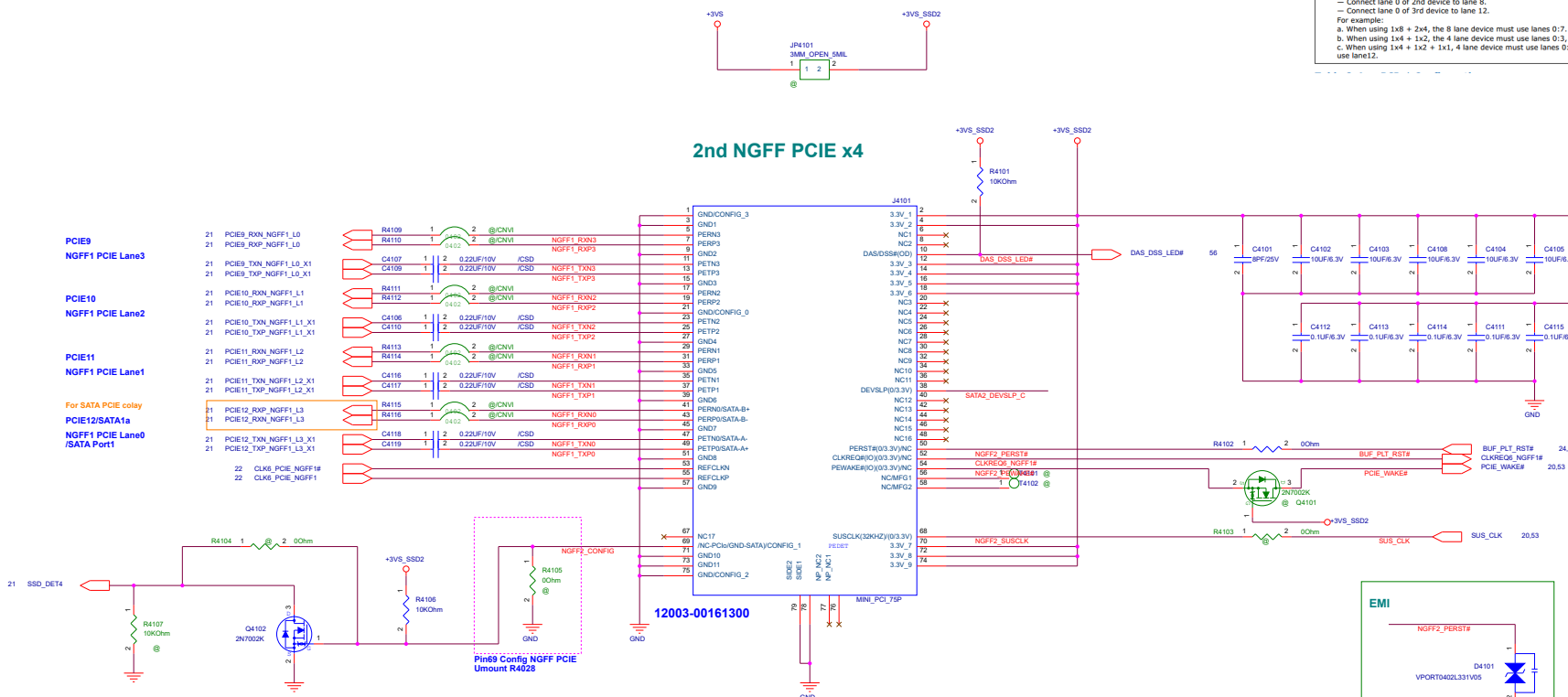
Option	NGFF2_CONFIG	SSD_DET4
PCIe SSD	1	0
SATA SSD	0	1

Table 8-3. Few Supported Normal and Lane-reversed Bifurcation Configurations

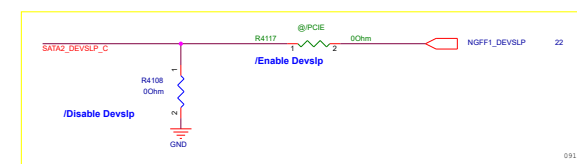
				Physical Lanes															
x16 Controller Negotiated Width	x8 Controller Negotiated Width	x4 Controller Negotiated Width	Processor	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x16	Off	Off	Direct	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
x8	x8	Off	Direct	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
x8	x4	x4	Direct	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3
x16	Off	Reverse	Reverse	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x8	x8	Off	Reverse	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
x8	x4	x4	Reverse	3	2	1	0	3	2	1	0	7	6	5	4	3	2	1	0

Notes:

- Support is also provided for narrow width and use devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to lane 0.
 - Connect lane 0 of 2nd device to lane 8.
 - Connect lane 0 of 3rd device to lane 12.
 For example:
 - a. When using 1x8 + 2x4, the 8 lane device must use lanes 0:7.
 - b. When using 1x4 + 1x2, the 4 lane device must use lanes 0:3, and other 2 lanes device must use lanes 8:9.
 - c. When using 1x4 + 1x2 + 1x1, 4 lane device must use lanes 0:3, two lane device must use lanes 8:9, one lane device must use lane 12.


2nd NGFF PCIe x4

Option	NGFF2_CONFIG	SSD_DET4
PCIe SSD	1	0
SATA SSD	0	1

HW_Control NGFF Device Sleep

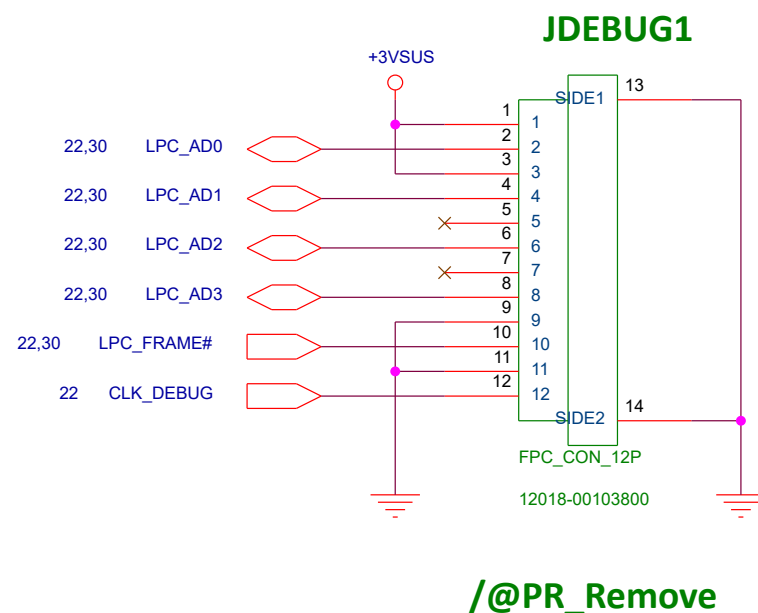
Close to Device connector

<Core Design>

		Title : HDMI_DP_Switch	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 42 of 103	

LPC Debug Port

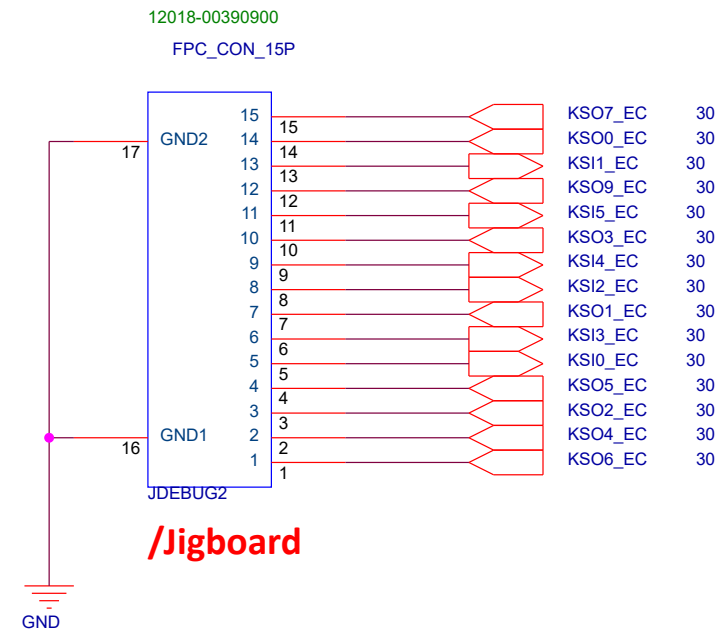
2017/11/10




1st: 12018-00103800
2nd :12018-00103300

2017/11/10

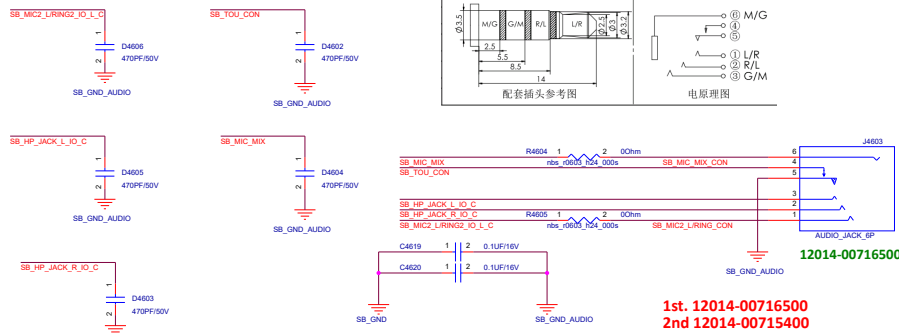
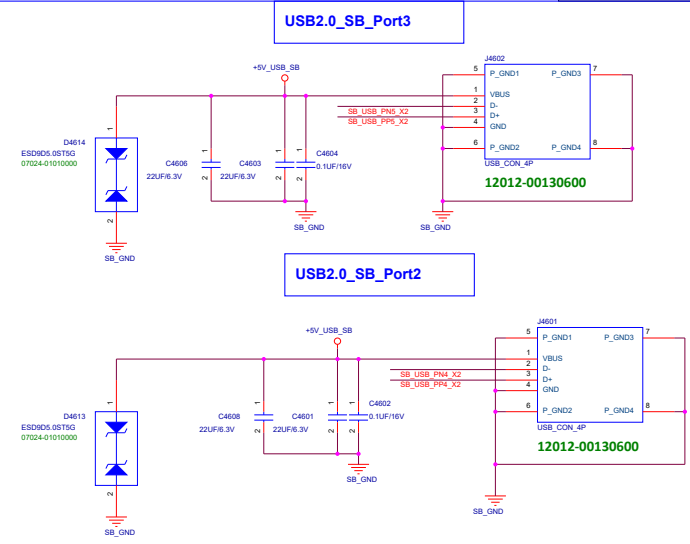
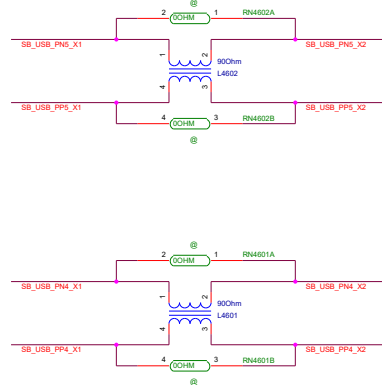
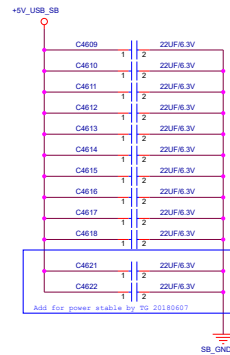
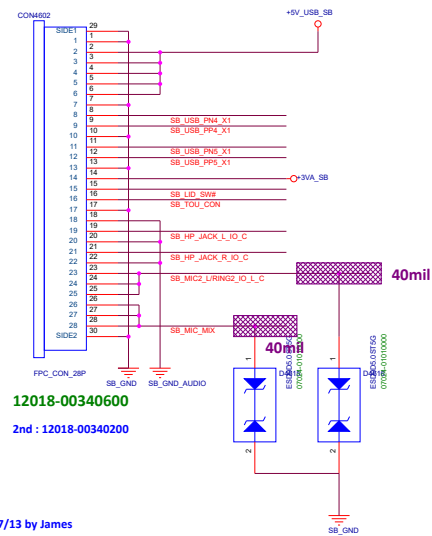
Flash BIOS



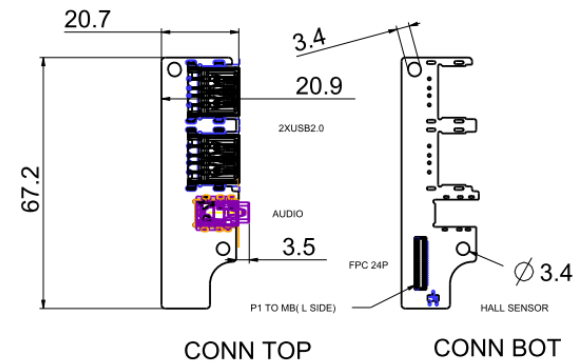
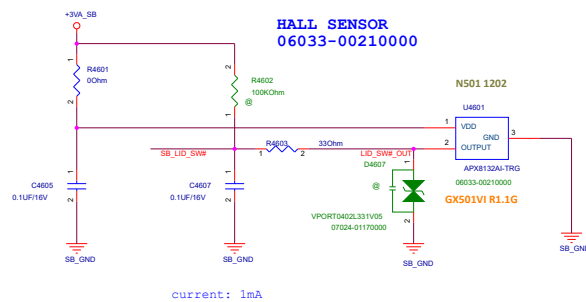
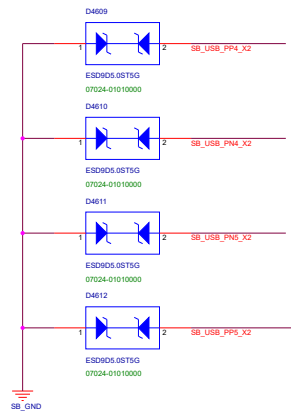
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		Title : DEBUG_LPC	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018	Sheet	44 of	103

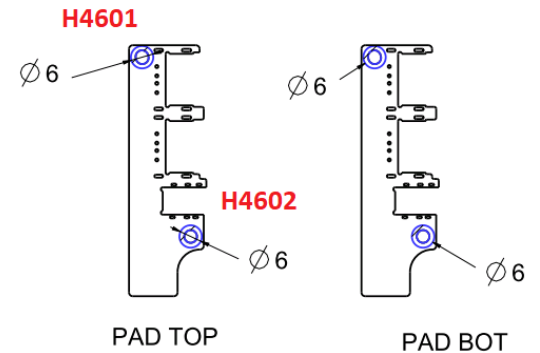
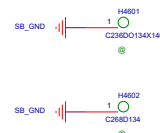
Connect to Page38

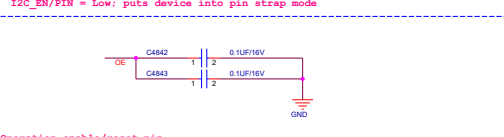
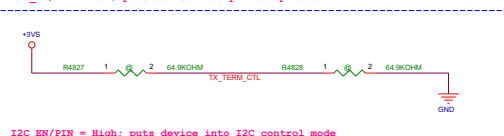
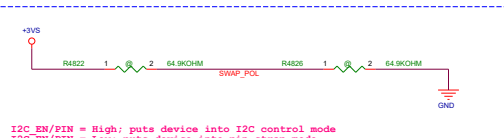
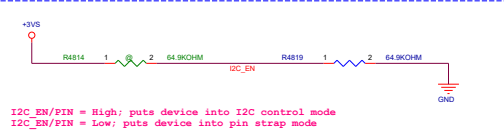
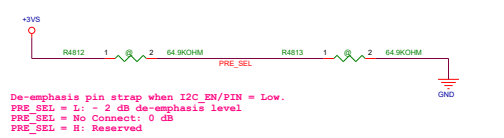
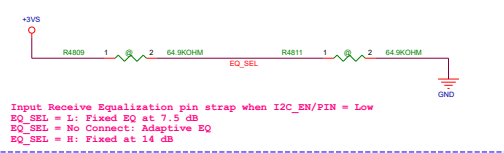
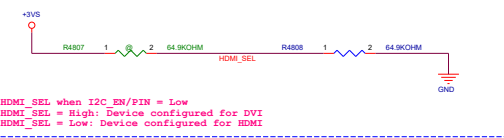
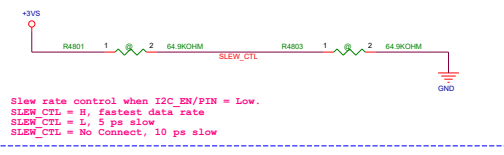


1st. 12014-00716500
2nd 12014-00715400

USB2.0
ESD-Protection

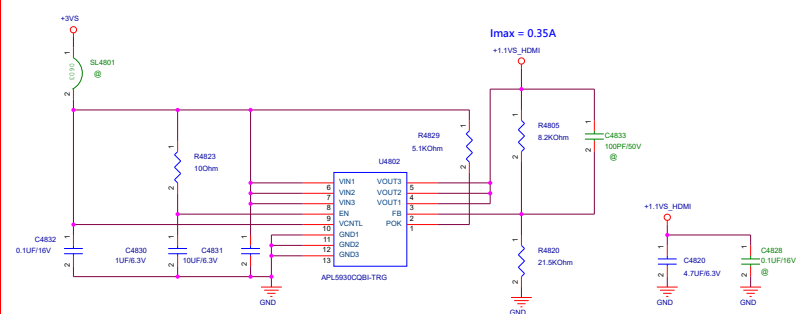
Screw





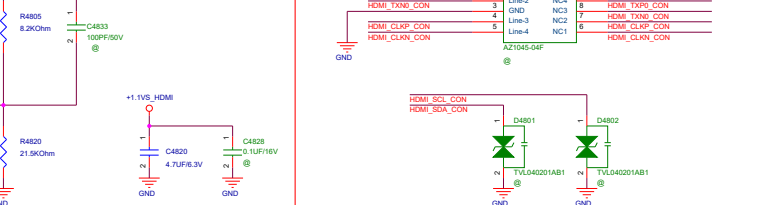
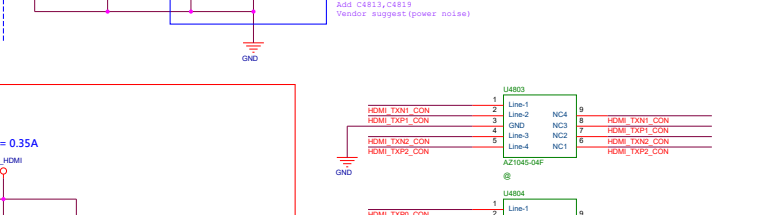
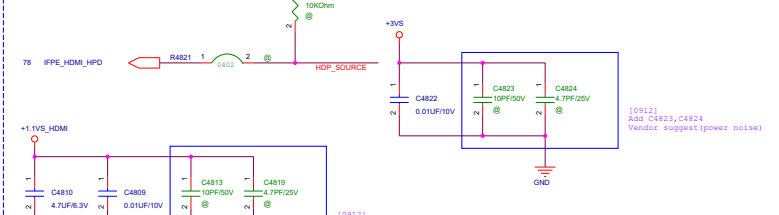
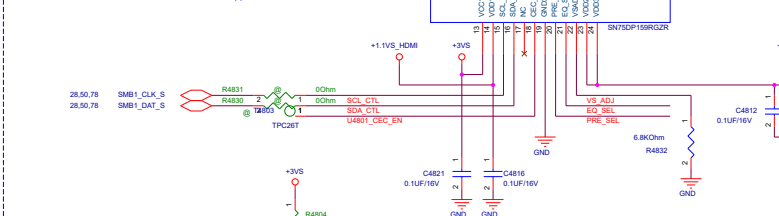
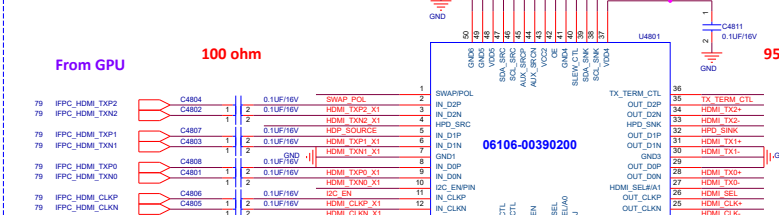
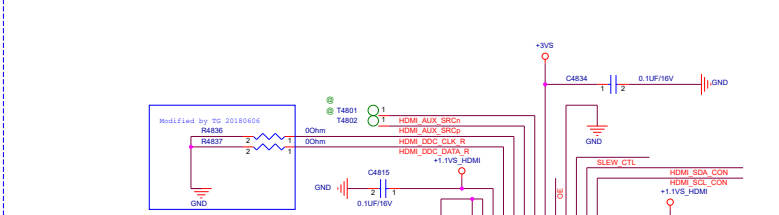
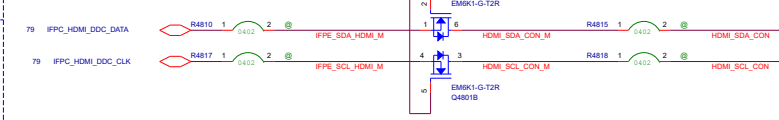
Operation enable/reset pin
OE = L: Power-down mode OE = H: Normal operation
Internal weak pullup: Resets device when transitions from H to L

HDMI LDO 1.1VS

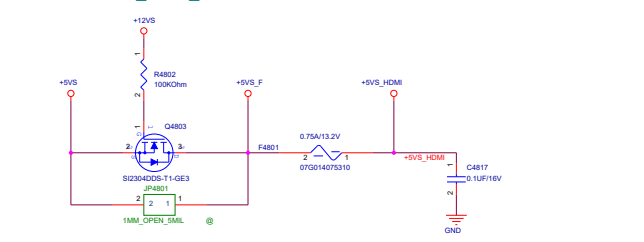


HDMI Active-Level Shift

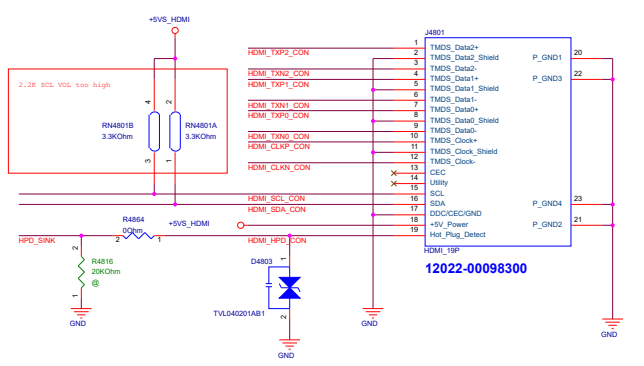
to GPU



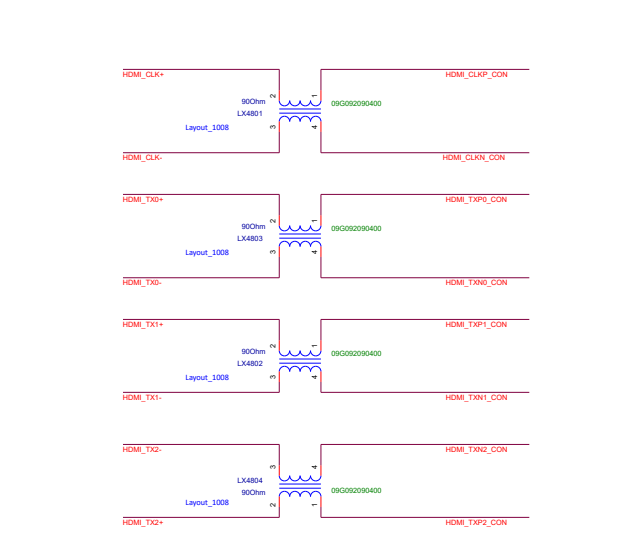
HDMI PWR_+5VS_HDMI

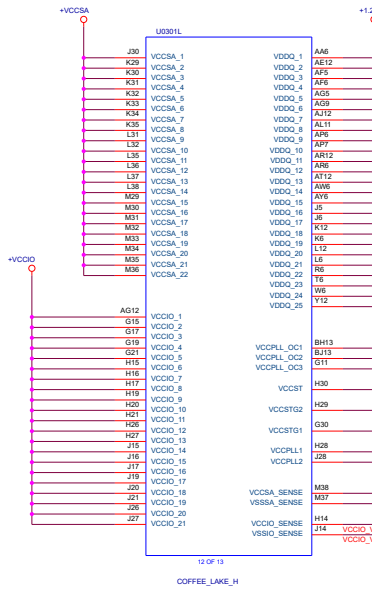


HDMI Conn.



HDMI EMI

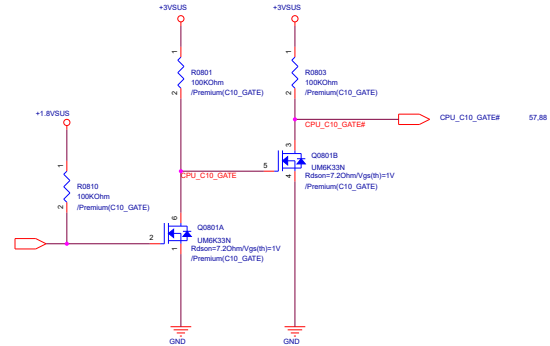


I_{max}=1.05V/11.1AI_{max}=1.2V/3.3A

Domain	Board Edge cap	Backside cap	Notes
Vcc _{ST}		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route Vcc _{ST} closest adjacent layer over any power net other than ground.
Vcc _{STG}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail.
Vcc _{PLL}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
		1x 22uF/47uF 0805 (placeholder)	*Placeholder not stuffed. To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.
Vcc _{PLL_OC}		2x 1uF 0201	Must be Ground referenced. Share with Vcc _Q . Board resistance from BGA to Power gate should be less than 86mOhm.

Domain	Board Edge cap	Backside cap	Notes
Vcc _{SA}	2x 47uF 0805 2x 22uF 0603		
Vdd _Q		7x 10uF 0402 1x 1uF 0201 4x 22uF 0603 11x 10uF 0402	
Vcc _{IO}		3x 10uF 0402	Additional capacitors might be needed if the connectivity from BGAs to capacitors is not adequate.
Vcc _{ST}		1x 1uF 0201	Must be Ground referenced. Board routing resistance from BGA to Power gate should be less than 10mOhm. Do not route Vcc _{ST} closest adjacent layer over any power net other than ground.
Vcc _{STG}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail.
Vcc _{PLL}		1x 1uF 0201	Must be Ground referenced. Share with 1.0V PCH rail. Board resistance from BGA to Power gate should be less than 130mOhm.
		1x 22uF/47uF 0805 (placeholder)	*Placeholder not stuffed. To be placed as close as possible to BGA (H28, J28) and be placed either at board edge or backside.
Vcc _{PLL_OC}		2x 1uF 0201	Must be Ground referenced. Share with Vcc _Q . Board resistance from BGA to Power gate should be less than 86mOhm.

24 CPU_C10_GATE#_PCH



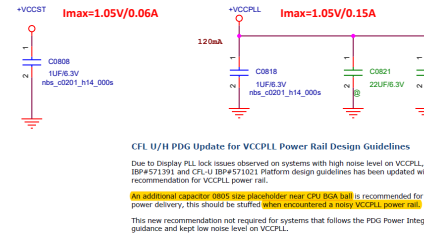
Configuration		Estimated SoC Power Delta from Config #1 to #2
Config #1 (Premium)	Config #2 (Volume)	CFL H
Vcc _{ST} off in S3	On in S3	+25-30mW
Vcc _{PLL_OC} off in S0/C10	On in S0/C10	+3-10mW
Vcc _{PLL_OC} off in S0ix	On in S0ix	+3-10mW

Other than what is documented in the table above, there is no expected SoC power delta in Sx states between Volume and Premium configurations. Independently, implementing Deep Sx (also known as DSW) may lower platform power over traditional Sx.

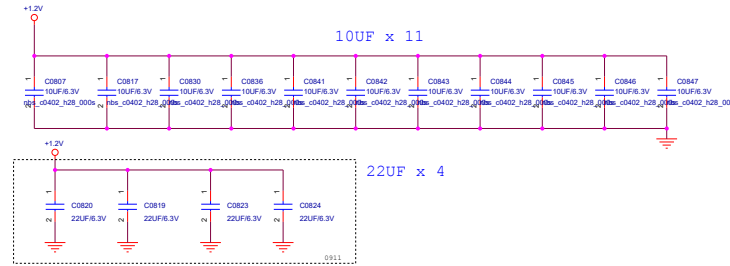
CPU_C10_GATE# is a signal from the Coffee Lake SoC that can be used for gating off Vcc_{STG}, Vcc_{PLL_OC} and Vcc_{IO} (CFL-H) in the S0/C10 system state in order to save power.

Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.05VSUS	+VCCST	
	+1.2V	+VCCSTG	
	+VCCSA	+VTT	
	+VCCIO	+VCCPLL_OC	

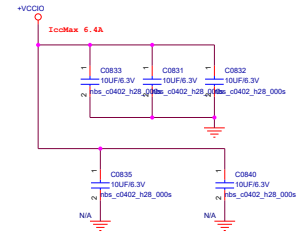
+VCCST/+VCCPLL DECAPS Place Back Side (TOP)



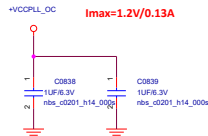
+VDDQ DECAPS Place Back Side (TOP)

I_{max}=1.2V/3.3A

+VCCIO DECAPS Place Back Side (TOP)

I_{max}=0.95V/6.4A

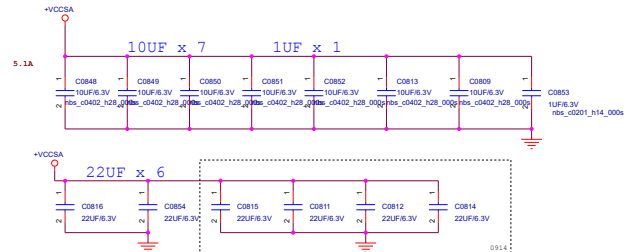
+VCCPLL_OC DECAPS Place Back Side (TOP)



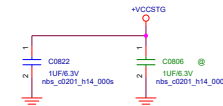
+VCCSA DECAPS Place Back Side (TOP)

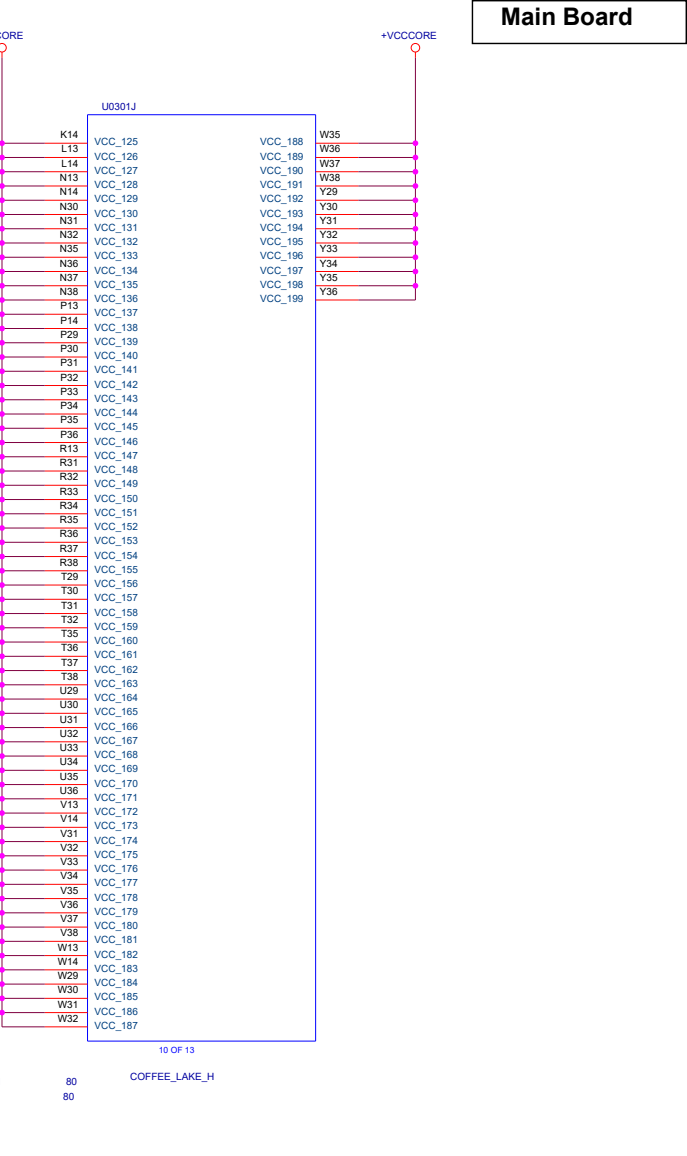
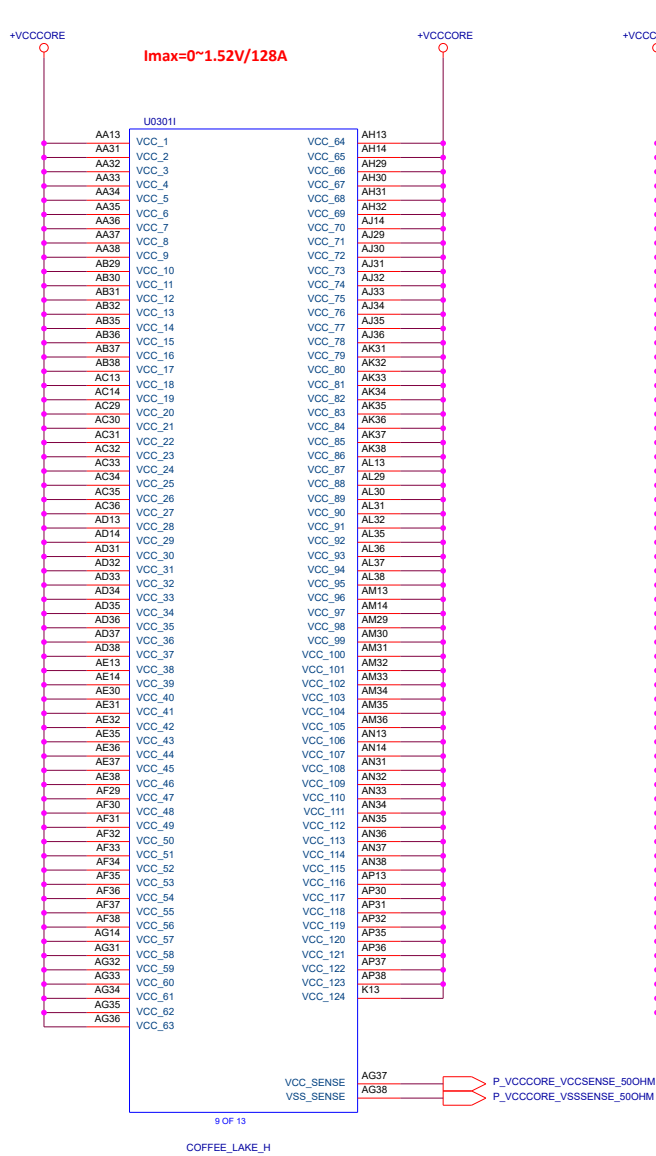
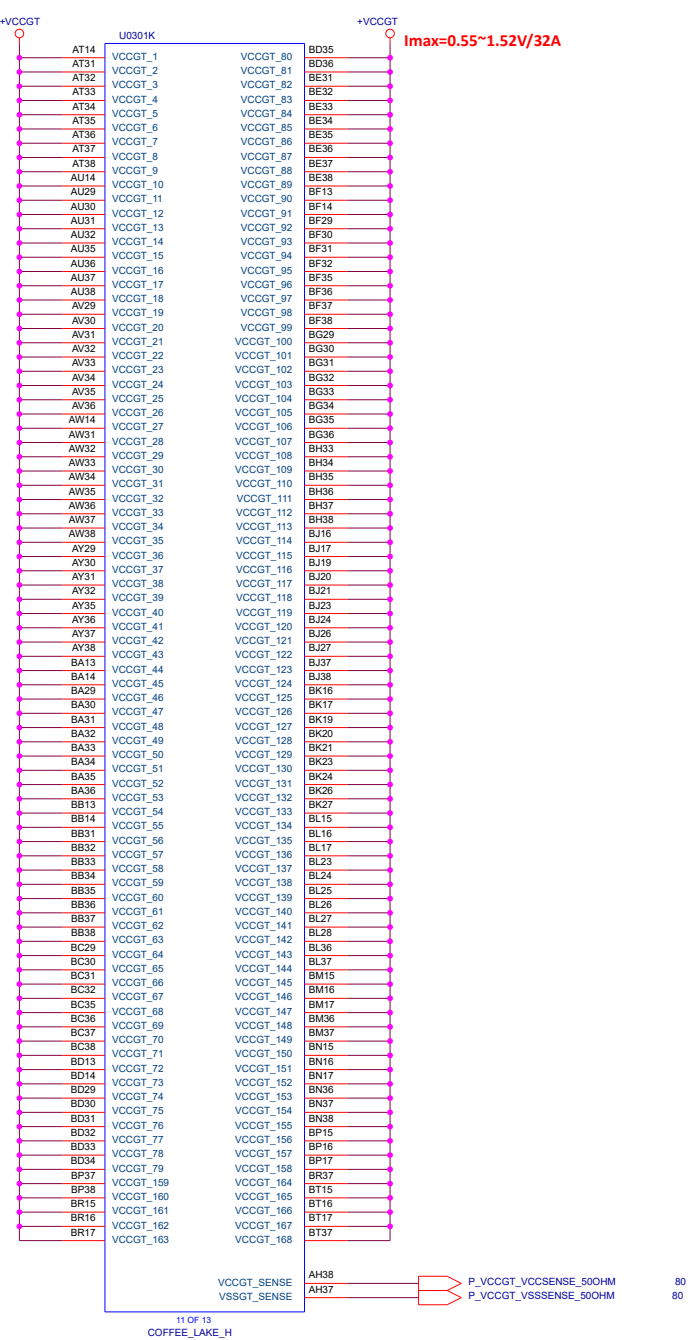
I_{max}=1.05V/11.1A

+VCCSA near CPU

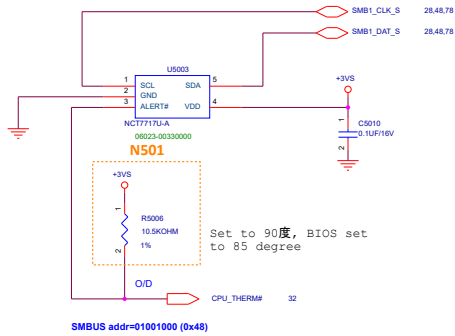


+VCCSTG DECAPS Place Back Side (TOP)



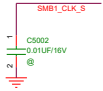


CPU Thermal Sensor



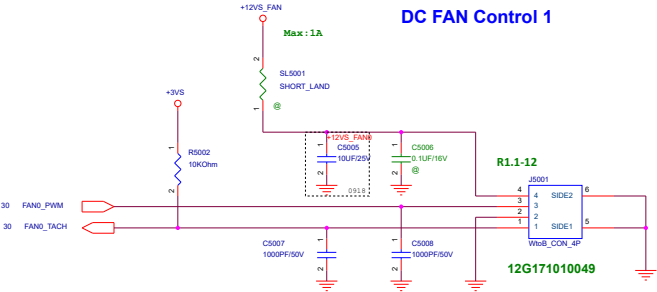
Temp.	Resistor
75	2kOhm
90	7.5kOhm
100	10.5kOhm
105	14kOhm
110	18.7kOhm

Reserve for
powr noise



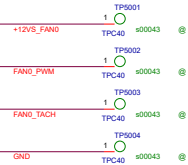
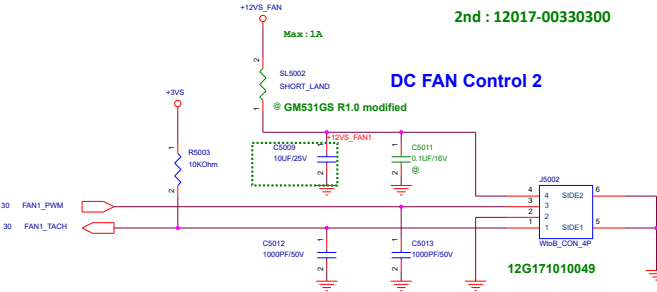
06G023123010為RD不建議用料: 此為舊版, 建議改用新板(cost低)06023-00330000/NCT7717U-A。

DC FAN Control 1

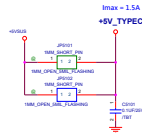


2nd : 12017-00330300

DC FAN Control 2

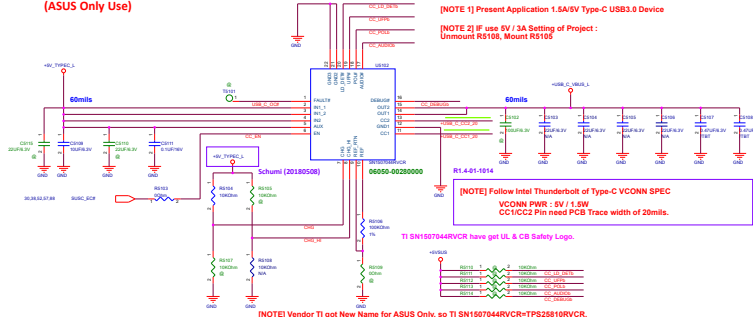


<Core Design>



TI CC Logic SN1507044RVCR = TPS25810RVCR, DFP (Host), 5V / 1.5A

(ASUS Only Use)



[NOTE 1] Present Application 1.5A/5V Type-C USB3.0 Device

[NOTE 2] If use 5V / 1A Setting of Project : Unmount R5108, Mount R5105

[NOTE] Follow Intel Thunderbolt of Type-C VCONN SPEC VCONN PWR : 5V / 1.5W CC1CC2 Pin need PCB Trace width of 20mils.

TI SN1507044RVCR have get UL & CB Safety Logo.

[NOTE] Vendor TI got New Name for ASUS Only, so TI SN1507044RVCR=TPS25810RVCR. Please Follow Design IP : TYPE-C CC Logic IC need use PIN-06050-00280000 TI/SN1507044RVCR

Set CC I limit = 3A

Table 3. USB Type-C Current Advertisement

CHG	CHG_HII	CC CAPABILITY BROADCAST	CURRENT LIMIT (typ)	LOAD DETECT THRESHOLD (typ)
0	0	STD	1.7 A	NA
0	1	STD	1.7 A	NA
1	0	1.5 A	1.5 A	NA
1	1	3 A	3 A	100 mV

6.7.2 Thunderbolt VCONN Source Electrical Requirements

Table 6-3. Thunderbolt VCONN Source Electrical Requirements

Parameter	Description	Min	Typ	Max	Units	Note
Vbus_min	Minimum voltage provided by host to connector	4.75	5	5.5	V	7.5mA
Vbus_max	Maximum voltage provided by host to connector	4.75	5.5	5.5	V	1.5A min

3.5.3 VCONN Requirements

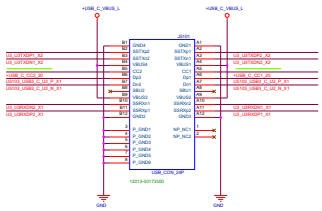
The Thunderbolt Active Cable shall be powered from VCONN not VBUS. The USB Type-C full featured active cable shall consume 3 W maximum from VCONN by default and 5.5W maximum from VCONN when in Thunderbolt or DisplayPort Alternate Modes. It shall be connected to VCONN on end connector. The Thunderbolt Active cable shall respond to S0P and S0P+ messages. The cable shall respond to S0P from the side of the cable which received VCONN from the USB Type-C connector. The cable responds to S0P+ from the side which does not receive VCONN. The cable shall continue to respond to S0P+ and S0P+ after a VCONN_Swap.

NOTE 8. PIN ASSIGNMENT (FRONT VIEW)

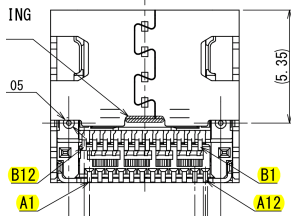
Pin No.	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
	GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2+	RX2-	GND
	GND	RX1+	RX1-	VBUS	SBU2	D+	D-	CC2	VBUS	TX2+	TX2-	GND
Pin No.	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

NOTE 9. LASER WELD POINTS MAY BE DISCOLORED.

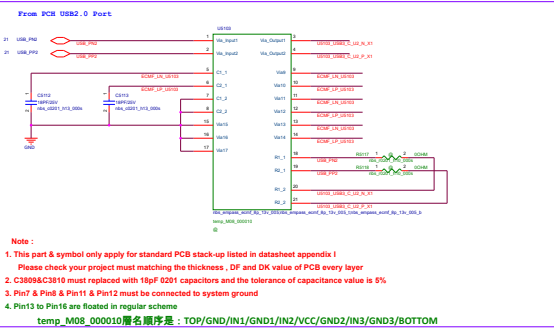
TYPE-C Connector



New PN : 12013-00173600



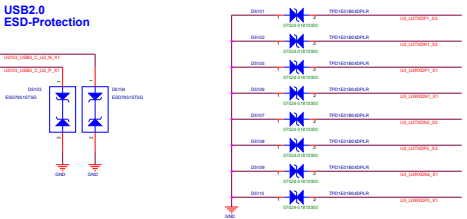
USB2.0 EMI-Protection With ECMF (PCB 1.05mm_10Layer)



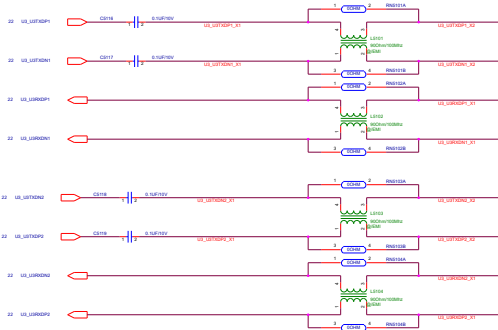
- Note : 1. This part & symbol only apply for standard PCB stack-up listed in datasheet appendix I Please check your project must matching the thickness , DF and DK value of PCB every layer 2. C3808&C3810 must replaced with 18pF 0201 capacitors and the tolerance of capacitance value is 5% 3. Pin7 & Pin8 & Pin11 & Pin12 must be connected to system ground 4. Pin13 to Pin16 are floated in regular scheme

temp_M08_000010層名順序是 : TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

USB3.0 ESD-Protection



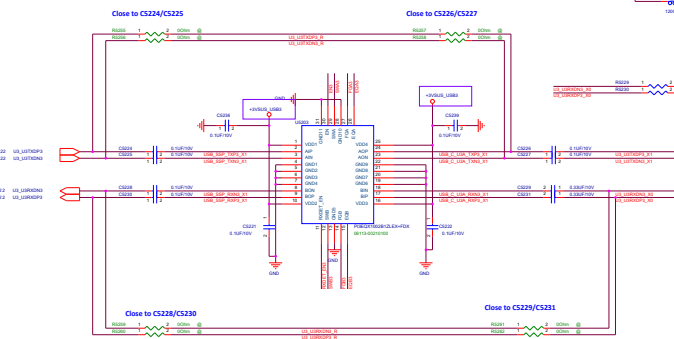
USB3.0 EMI-Protection



<Core Design>

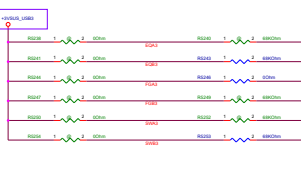
Pericom : 06113-00210000 REDRIVER IC P138CX1002R2LX

[Bypass Path]



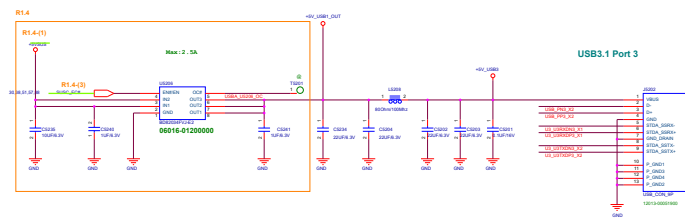
< Channel / Receiver setting for Pericom 1002B >

Setting	Channel Enable [IN]	Receiver Detection [MODET_IN]
0 : 0-D to GND	Disable	Disable
1 : 0-D to VDD	Enable(Default)	Enable(Default)
Note	Channel1 Enable / Receiver Detection With internal 300K pull-up R.	



5.PIN DEFINE TABLE:

PIN NO.	1	2	3	4	
SIGNAL NAME	VBUS	D-	D+	GND	
PIN NO.	5	6	7	8	9
SIGNAL NAME	StdA_SSRX-	StdA_SSRX+	GND-DRAIN	StdA_SSTX-	StdA_SSTX+



< Fine tune table for Pericom (One port Gen2) >

< EQ table for Pericom 1002B >

EQ[A-B]	Gen 1 @2.5Gbps(SB)	Gen 2 @2.5Gbps(SB)
0 : 0-D to GND	5.1	10.9
R : Read to GND	1.9	6.7
F : Leave Open	3.5(Default)	8.1(Default)
1 : 0-D to VDD	6.8	13.1

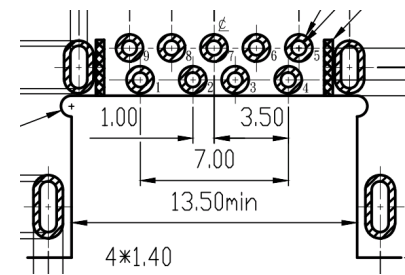
Note : With internal 100Kohm pull-up Res and 200Kohm pull-down Res.
Unit : dBattm

< FG table for Pericom 1002B >

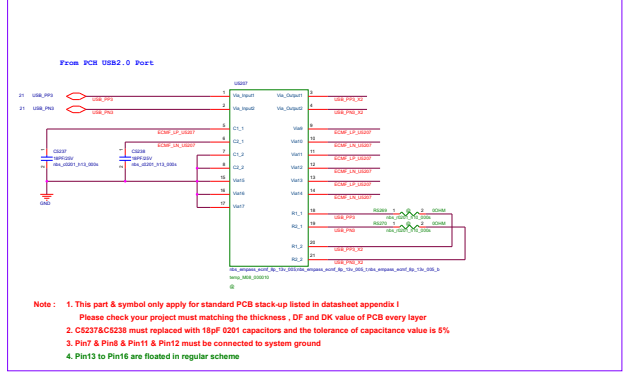
FG[A-B]	FGM Gain [dB]
0 : 0-D to GND	-3.0
R : Read to GND	-1.5
F : Leave Open	0 (Default)
1 : 0-D to VDD	+2.0

< SW table for Pericom 1002B >

SW[A-B]	Output Linear Scaling [dB]
0 : 0-D to GND	800
R : Read to GND	1300
F : Leave Open	1000 (Default)
1 : 0-D to VDD	1300

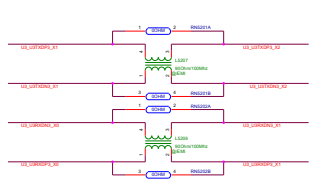


R1.5 USB2.0 EMI-Protection With ECMF(PCB 1.05mm_10Layer)

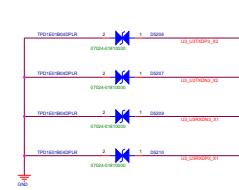


temp_M08_000010層名順序是 : TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

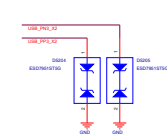
USB3.0 EMI-Protection



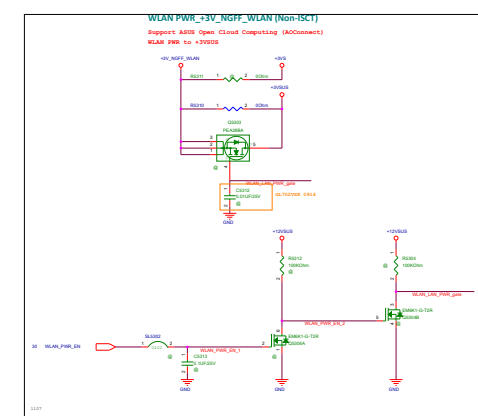
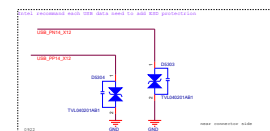
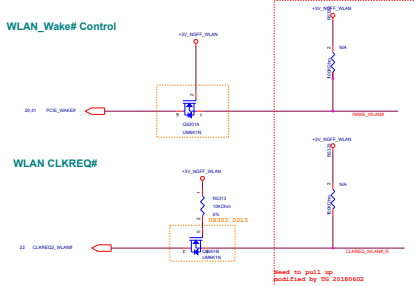
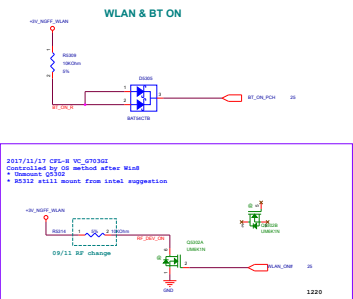
USB3.0 ESD-Protection



USB2.0 ESD-Protection

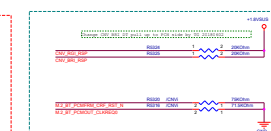
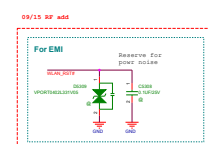
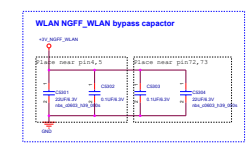
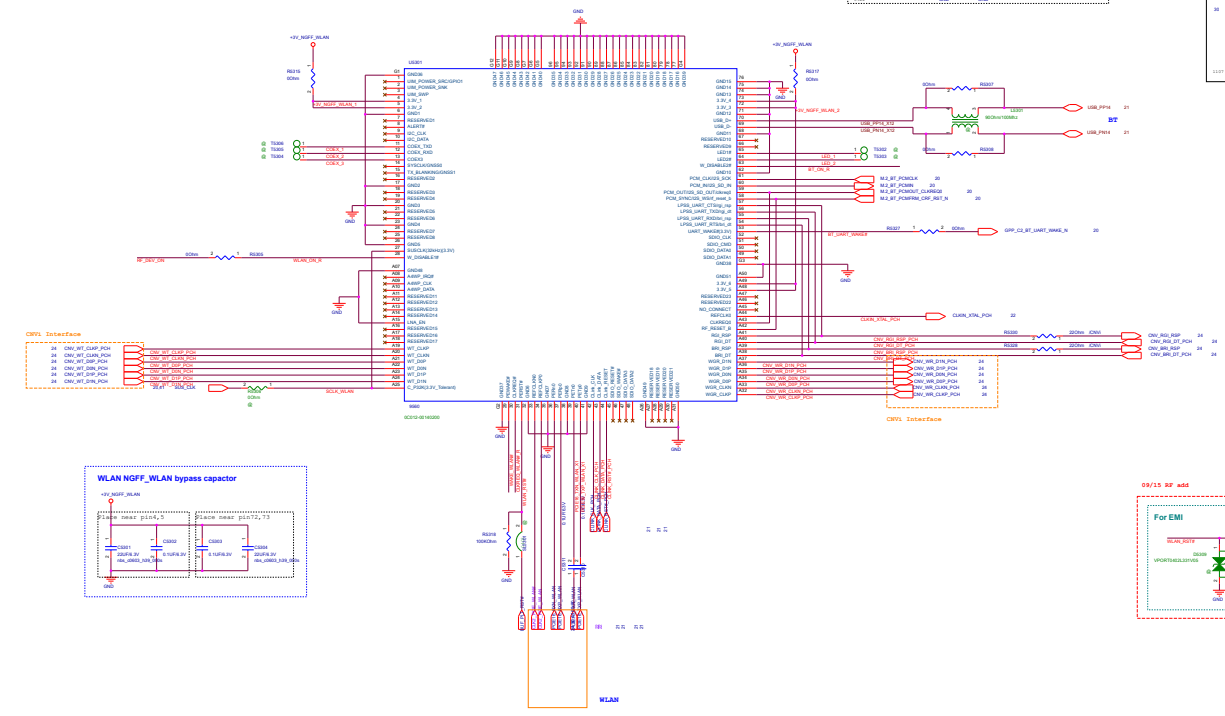


2017/11/23 Changed by James
Add D5204/D5205

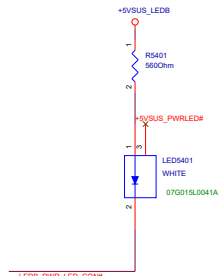
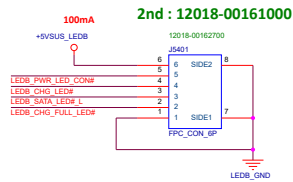


2017.03.15 Connector list update

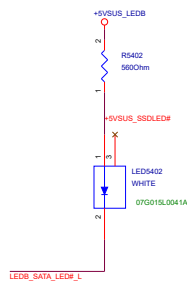
SD-1216



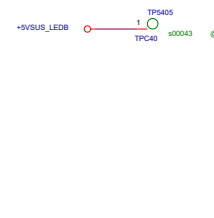
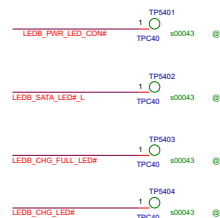
Side of PWR LED



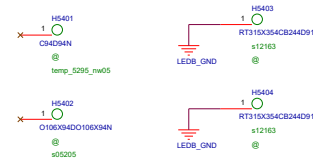
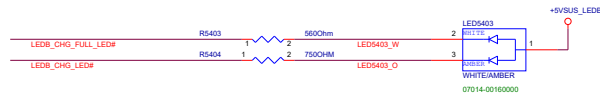
SSD LED



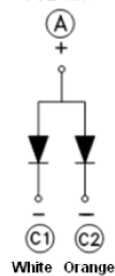
1st : Harvatek (07G015L0041A)
2nd : Liteon (07014-00474700)



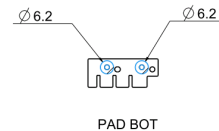
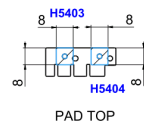
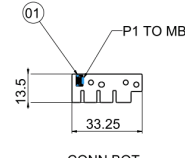
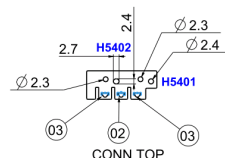
Charger LED



POLARITY



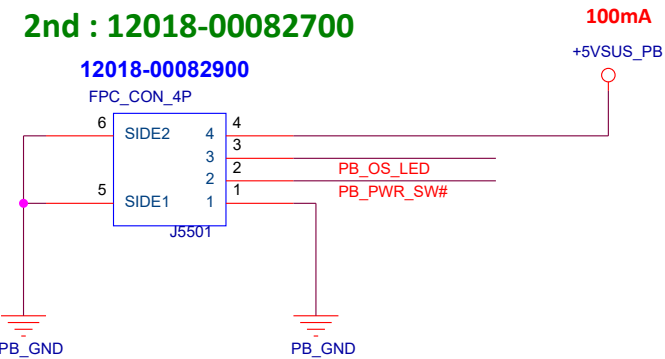
1st : Harvatek (07014-00160000)
2nd : Liteon (07014-00190300)



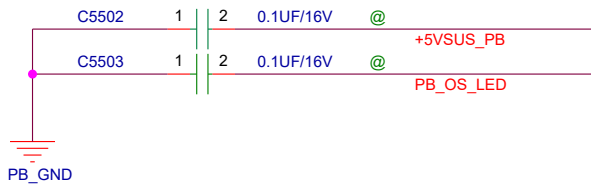
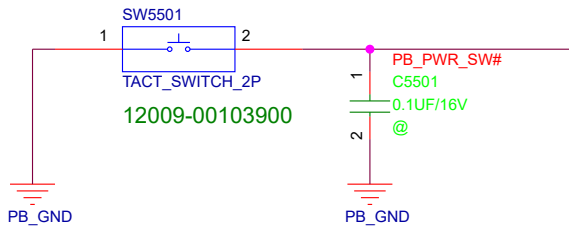
«Core Design»

ASUS		Title : USB3 *****	
ASUSTek COMPUTER INC		Engineer: EE	
Size	Project Name	Rev	
B	GX531GS	2.0	
Date: Thursday, July 19, 2018	Sheet	54	of 103

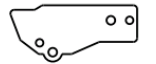
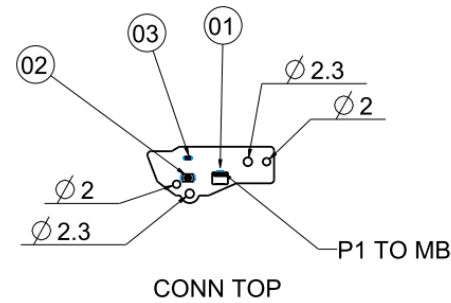
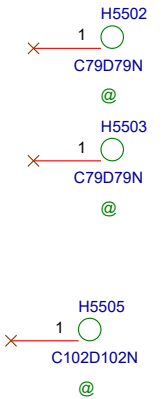
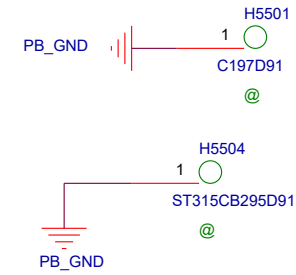
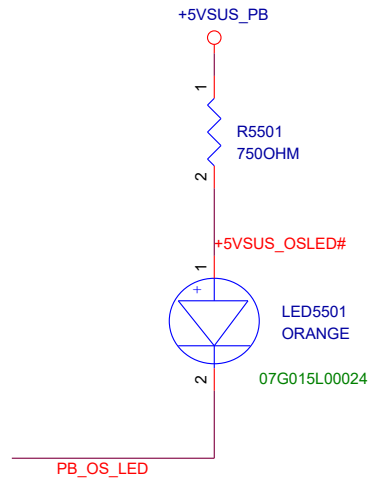
2nd : 12018-00082700



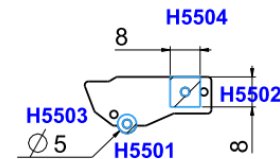
POWER button



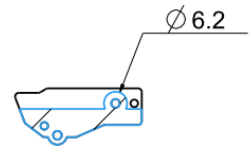
OS LED



CONN BOT



PAD TOP

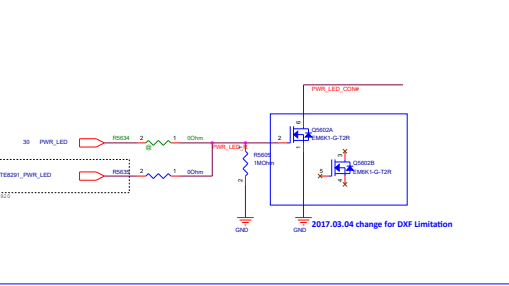


PAD BOT

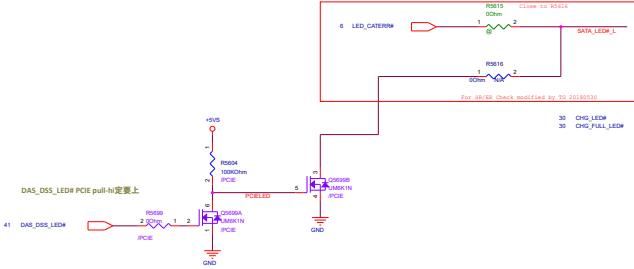
<Core Design>

ASUS		Title : IO Con. to MB	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018	Sheet	55 of 103	

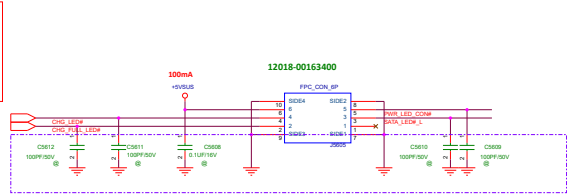
Side of PWR LED



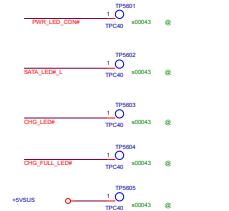
2014/05/29 Add HDD & SSD LED control circuit.



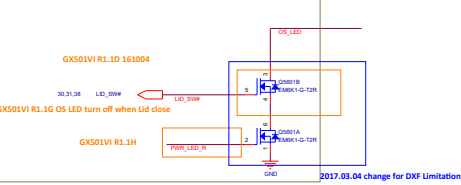
Connected to LED Board (Page 54)



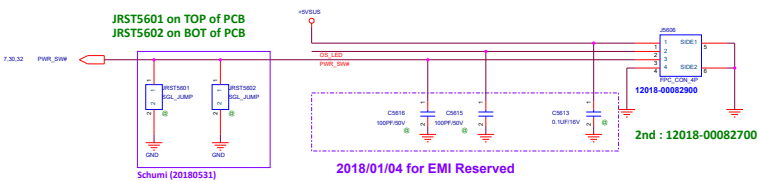
2018/01/04 for EMI Reserved



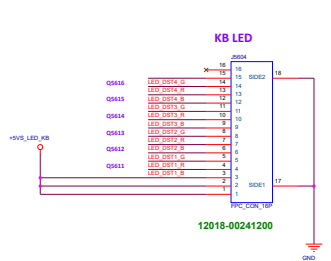
OS LED



Connected to Power Key Board (Page55)



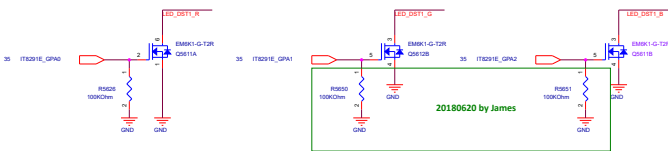
2nd : NC



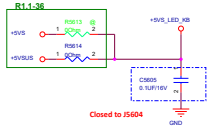
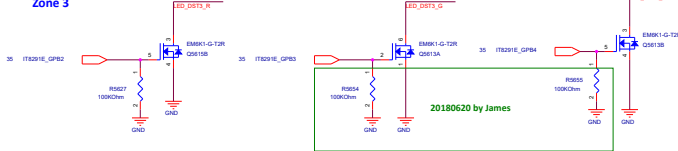
PIN 16	NC
PIN 15	Cathode LED4 green
PIN 14	Cathode LED4 red
PIN 13	Cathode LED4 blue
PIN 12	Cathode LED3 green
PIN 11	Cathode LED3 red
PIN 10	Cathode LED3 blue
PIN 9	Cathode LED2 green
PIN 8	Cathode LED2 red
PIN 7	Cathode LED2 blue
PIN 6	Cathode LED1 green
PIN 5	Cathode LED1 red
PIN 4	Cathode LED1 blue
PIN 3	vcc blue
PIN 2	vcc red
PIN 1	vcc green

KB RGB LED

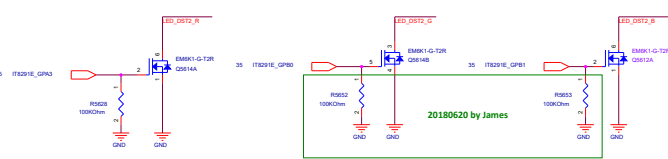
Zone 1



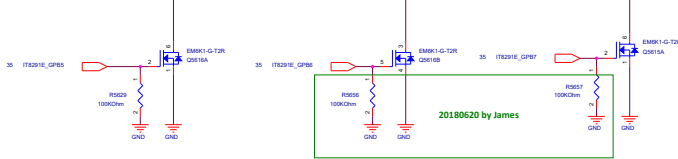
Zone 3



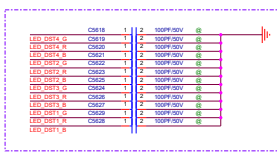
Zone 2



Zone 4

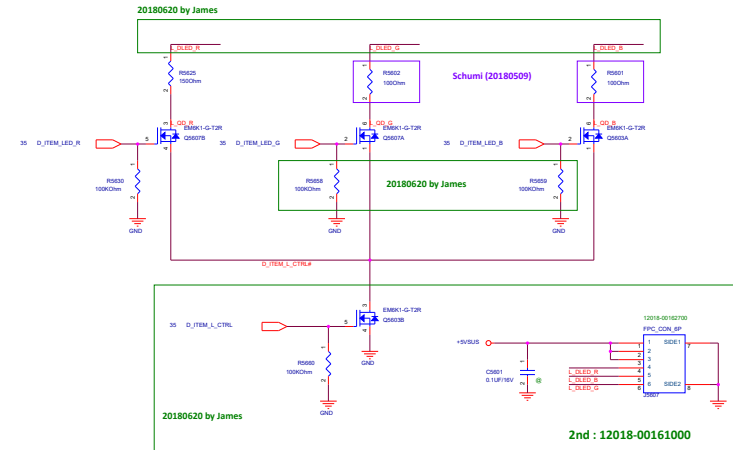


2018/01/04 for EMI Reserved

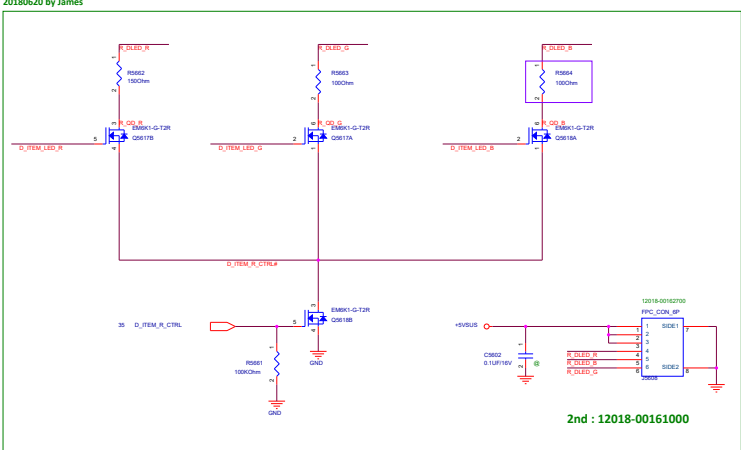


D item- RGB LED

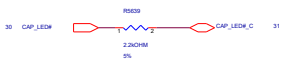
< D case LED L >

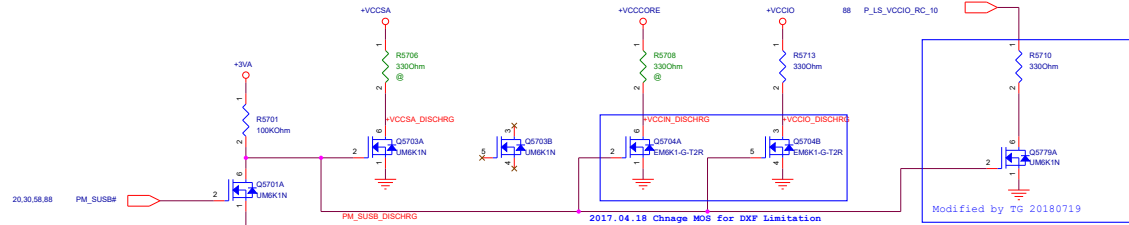


< D case LED R >

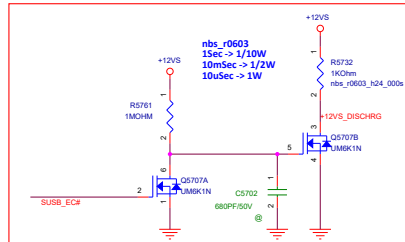
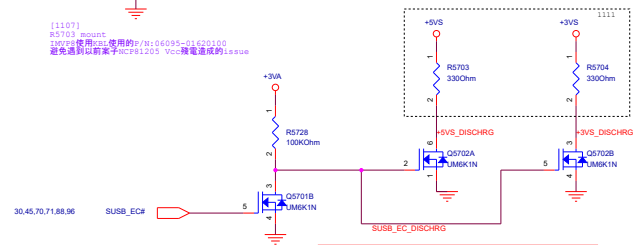


CAP LED

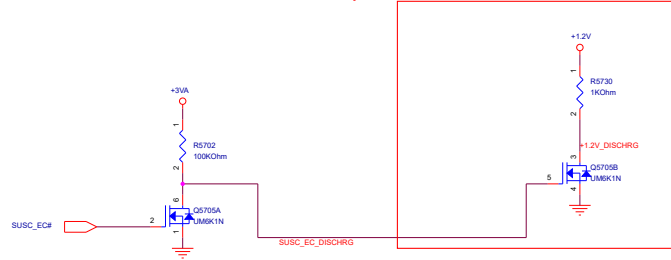




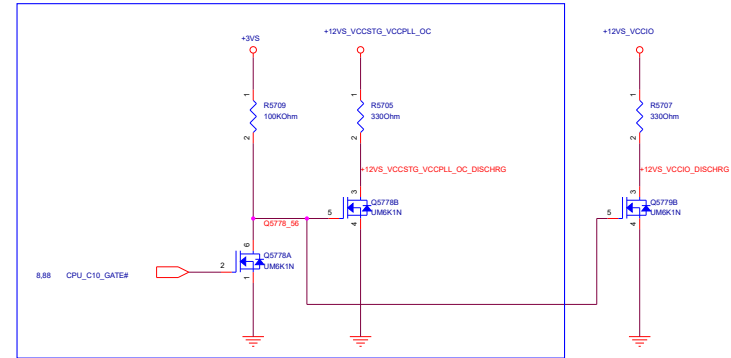
[1107]
R5703 mount
3V0P8使用xcl使用的P/N:06095-01620100
避免遇到以前案子中CP91205 Vcc殘電造成的Issue



SUSB_EC# turn off discharge before +12V ON
+12V turn on discharge after SUSB_EC# OFF



R1.1-13



<Core Design>

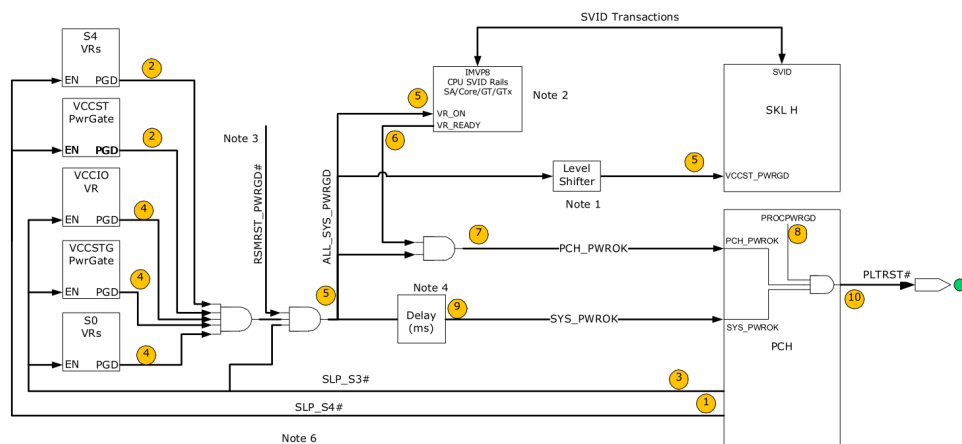
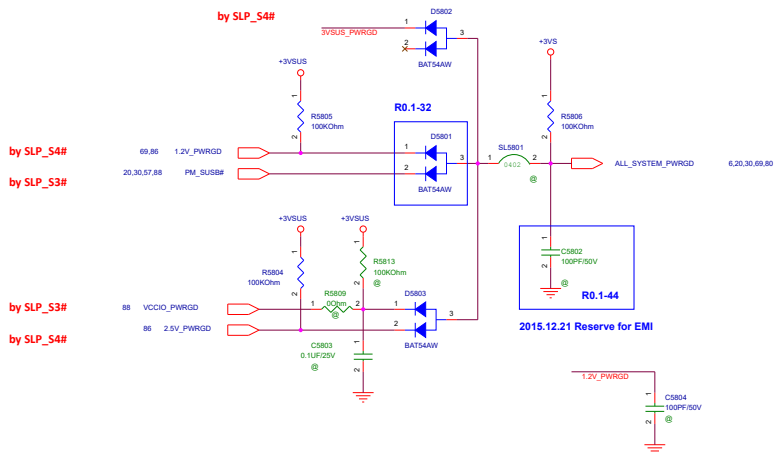
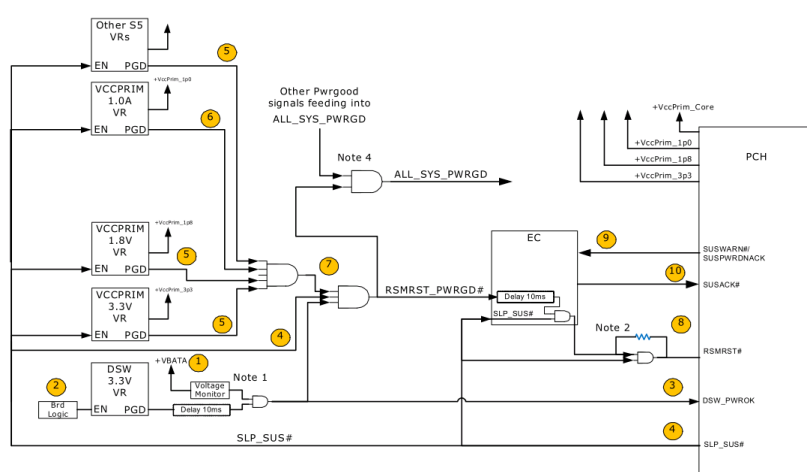
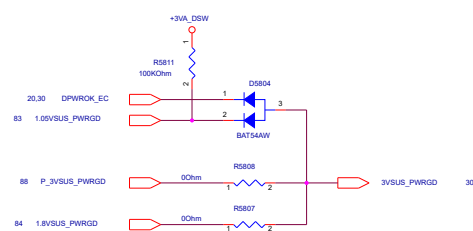
ASUS		Title : DSG_Discharge	
ASUSTek COMPUTER		Engineer: EE	
Size Custom	Project Name GX53IGS	Rev 2.0	
Date: Thursday, July 19, 2018	Sheet 57 of 103		

SUS_VR_PWRGD]

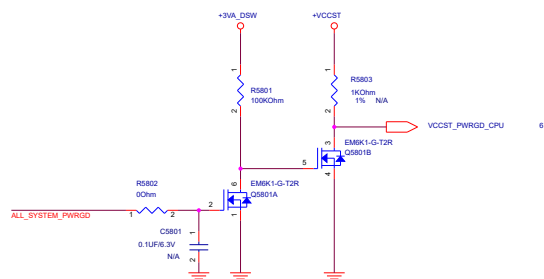
SLP_SUS_N
V0.85_PWRGD
V3.3A_VSA_PWRGD
V1.0A_PWRGD
V1.8A_PWRGD
DPWRGD=3.3A_DSWPWRGD+10ms & BATT>5.35V

[ALL_SYSTEM_PWRGD]


SLP_S3_N
DDR_PWRGD
VCCIO_PWRGD
3.35_MON
1.00U_MON
1.85_MON
RSMRST_PWRGD
SYS_PWROK



[VCCST_PWRGD for PCH]

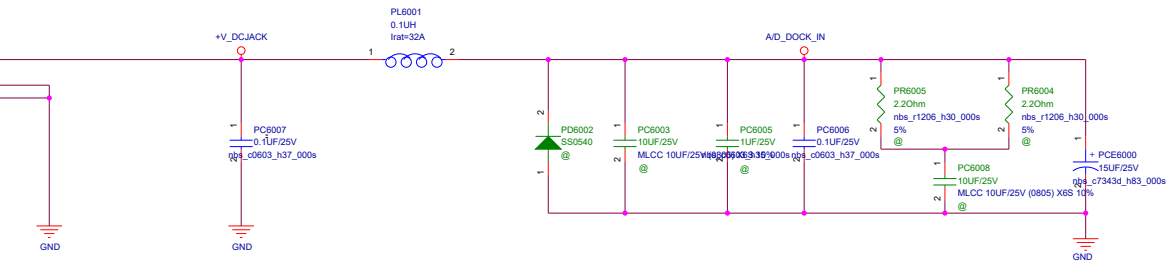
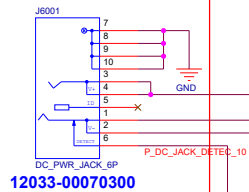


<Core Design>

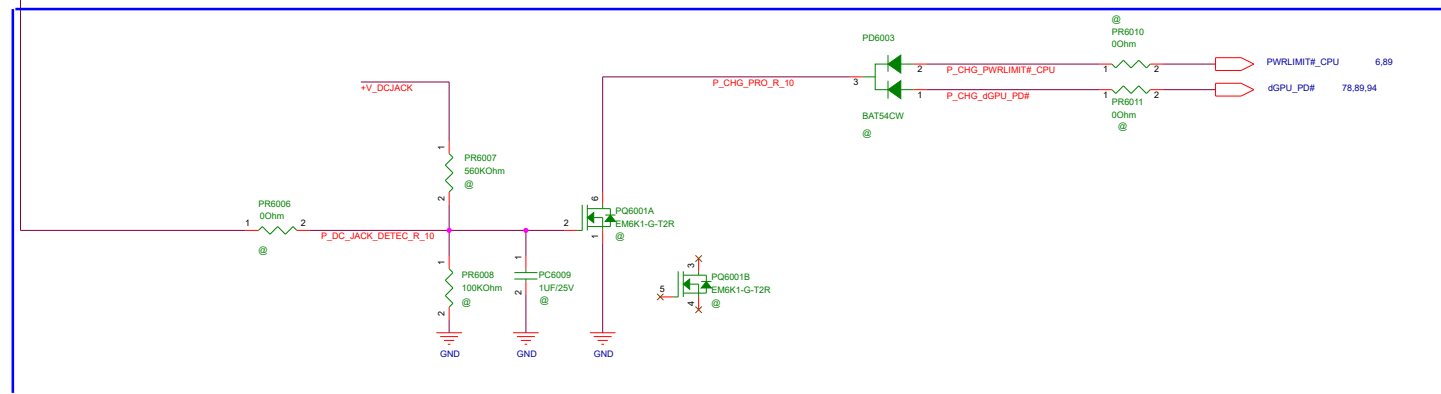
		Title : I/O_Main board Conn.	
ASUSTeK COMPUTER INC. NB3		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 59 of 103	

DC-IN Connector

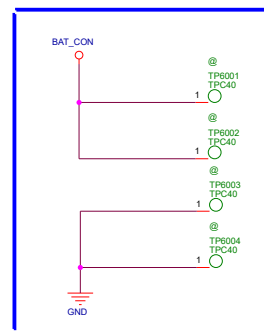
DC Jack使用請詢用River_Hsu



ER DC-JACK要由6Phi 2Pin(12033-00070300)改為6Phi 4Pin(12033-00020200),
該線路先斷開預留

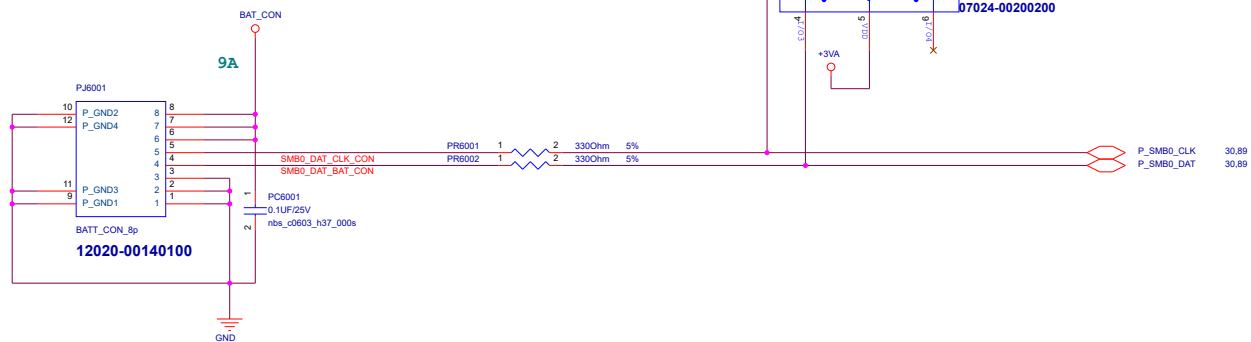


EE需求





Battery Connector


ESD Diode	P/N	Priority
AMAZING	07024-00200200	1
NXP	07024-00710000	2





Note: Battery Connector 正確性與BAT1_IN_OC#是否預留!

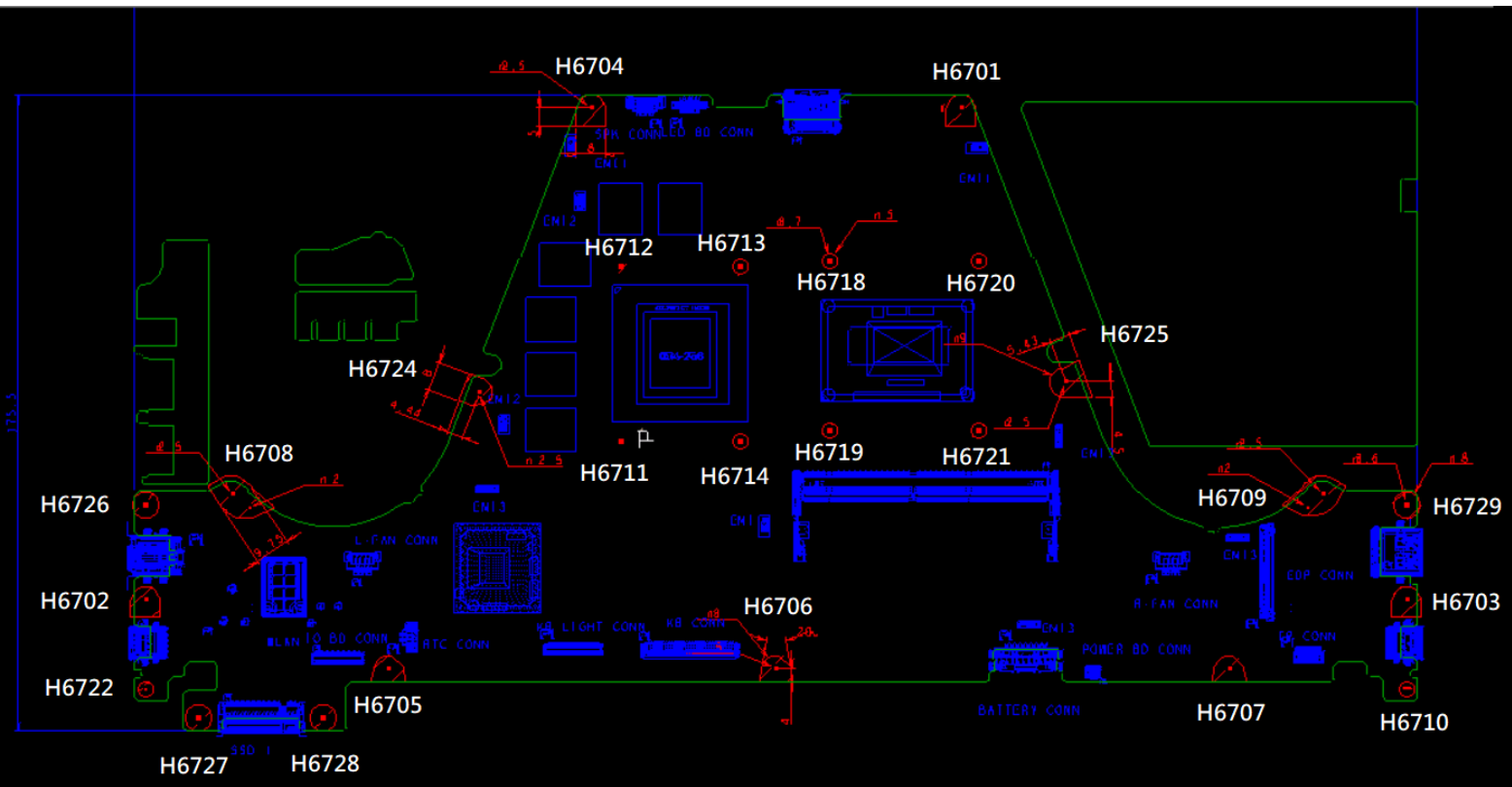
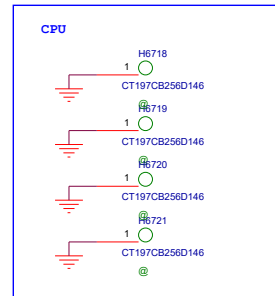
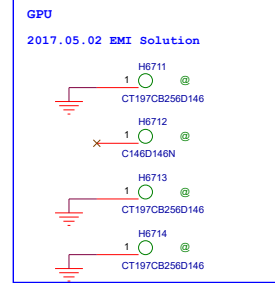
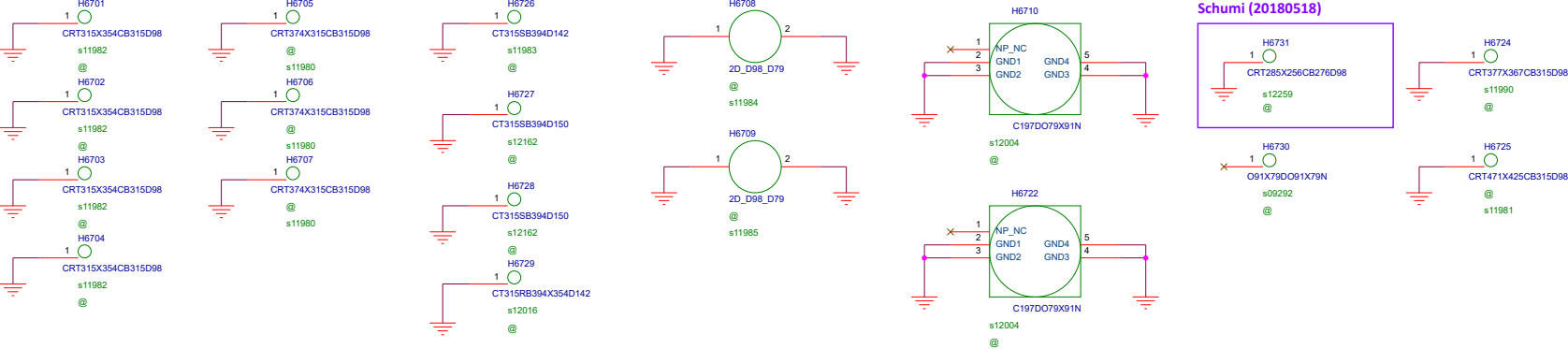
		Title : BT_Bluetooth	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 61 of 103	

		Title : I/O board(1-1)_CR_RTS5139	
ASUSTeK COMPUTER INC. NB3		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 62 of 103	

		Title : USB Port	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size A	Project Name GX531GS		Rev 2.0
Date: Thursday, July 19, 2018		Sheet 63 of 103	

		Title : ME_Screw Hole & Nut	
ASUSTeK COMPUTER INC. NB1		Engineer: EE	
Size	Project Name		Rev
A	GX531GS		2.0
Date: Thursday, July 19, 2018		Sheet 65 of 103	

			Title :		
ASUSTeK COMPUTER INC. NB1			Engineer: EE		
Size	Project Name				Rev
A	GX531GS				2.0
Date: Thursday, July 19, 2018			Sheet 66 of 103		



<Core Design>

ASUS		Title : I/O board FUNC key	
ASUSTek COMPUTER INC. NB3		Engineer: EE	
Size B	Project Name GX531GS	Rev 2.0	
Date: Thursday, July 19, 2018	Sheet	67	of 103



Title : OTH_for test only

ASUSTeK COMPUTER INC. NB1

Engineer: EE

Size

Project Name

Rev

A

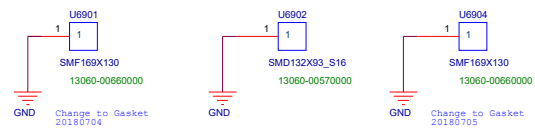
GX531GS

2.0

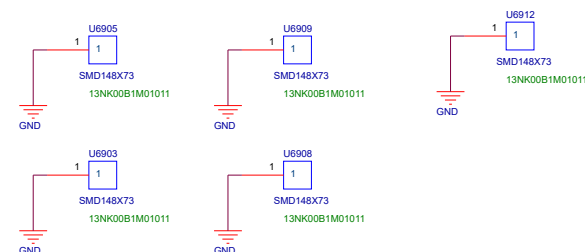
Date: Thursday, July 19, 2018

Sheet 68 of 103

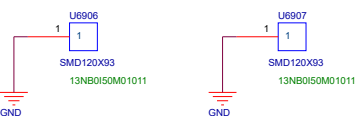
EMI1 SPRING (4.7H) *5
13060-00570000



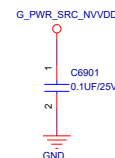
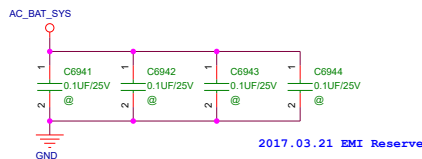
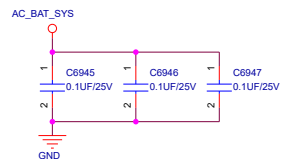
EMI2 SPRING (4H) *5
13NK00B1M01011



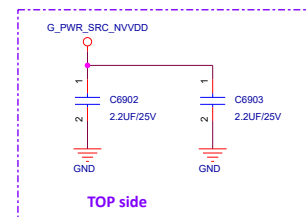
EMI2 SPRING (2.6H) *2
13NB0150M01011



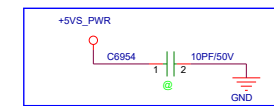
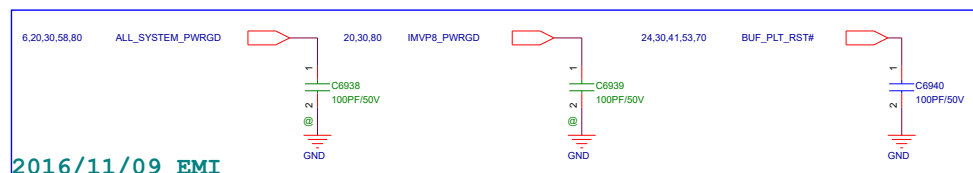
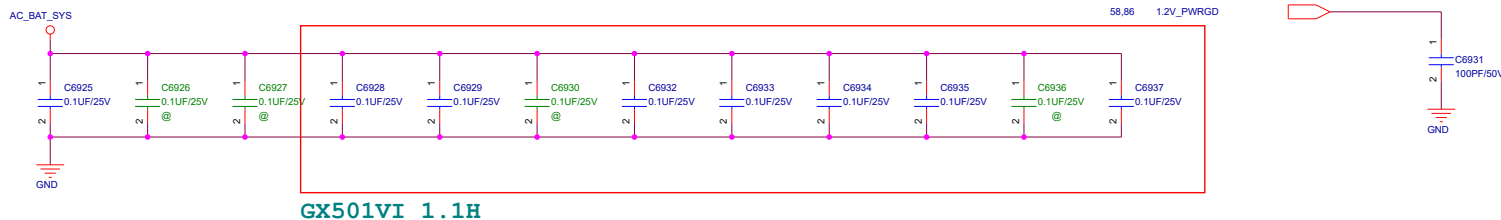
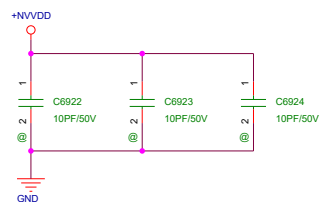
2017/04/05 EMI



4/2 for EMI

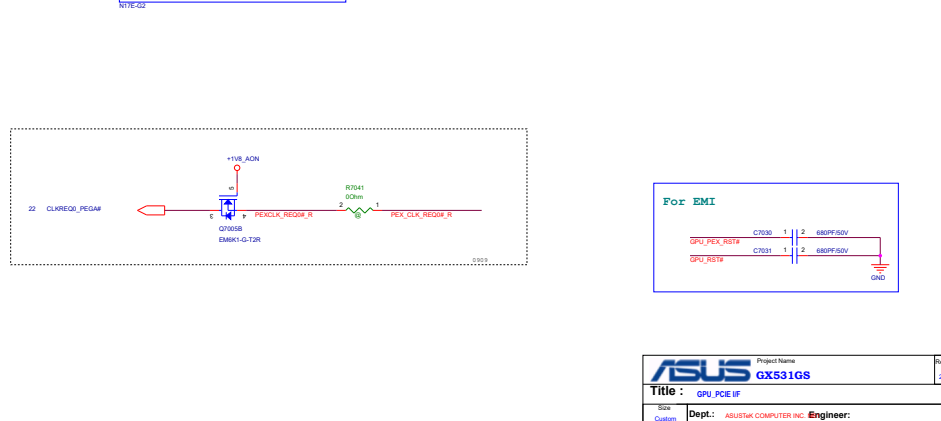
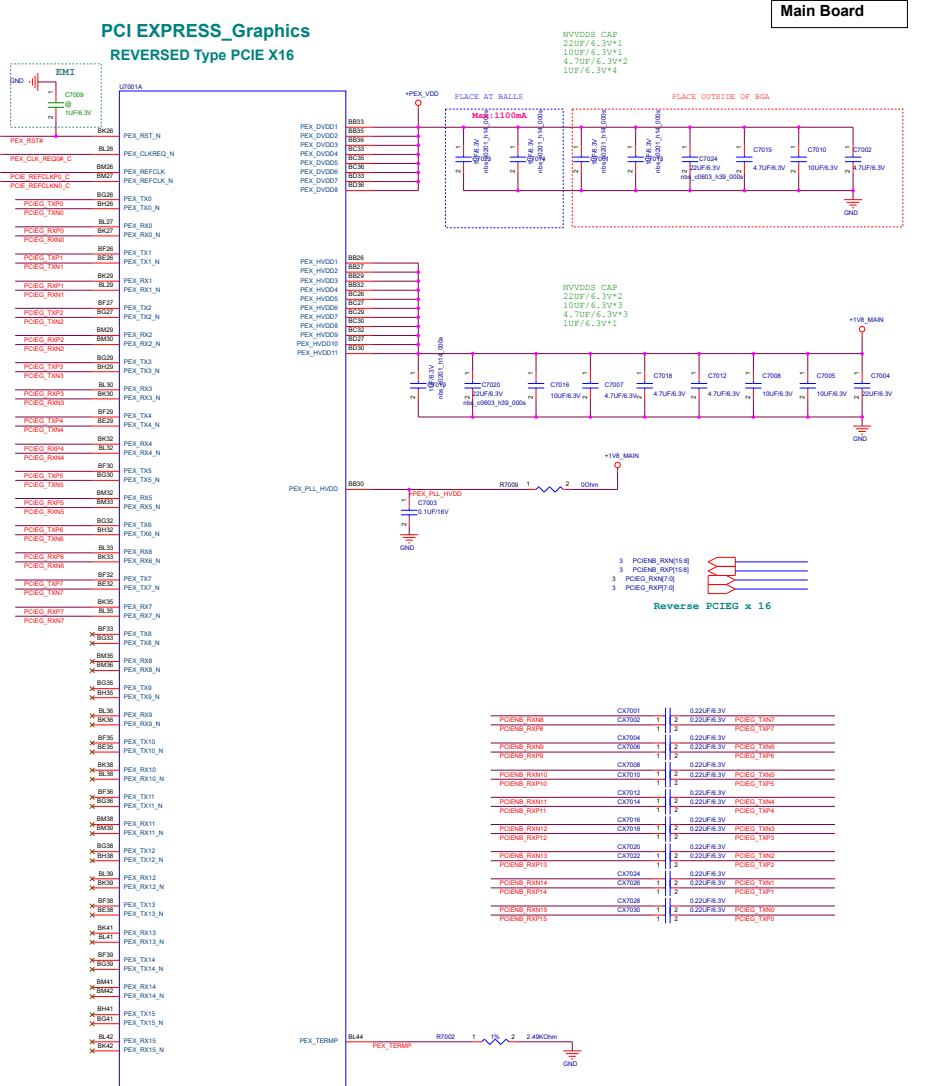
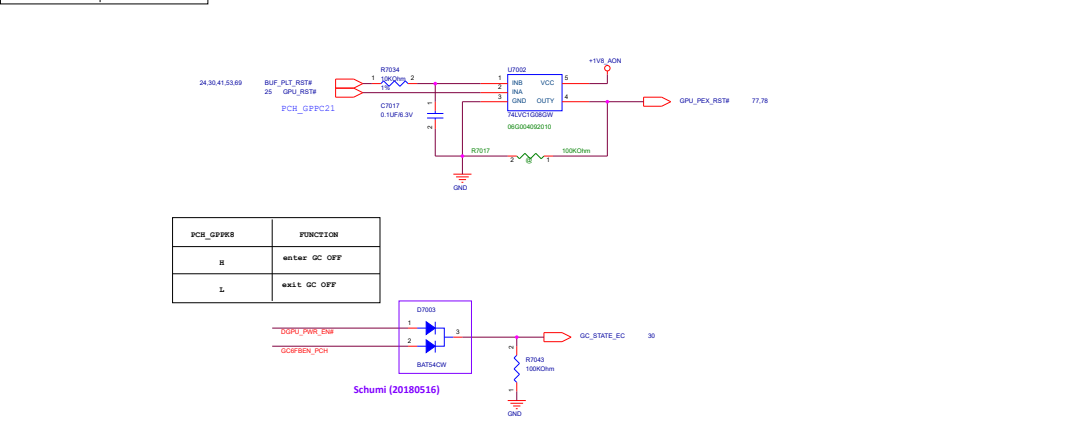
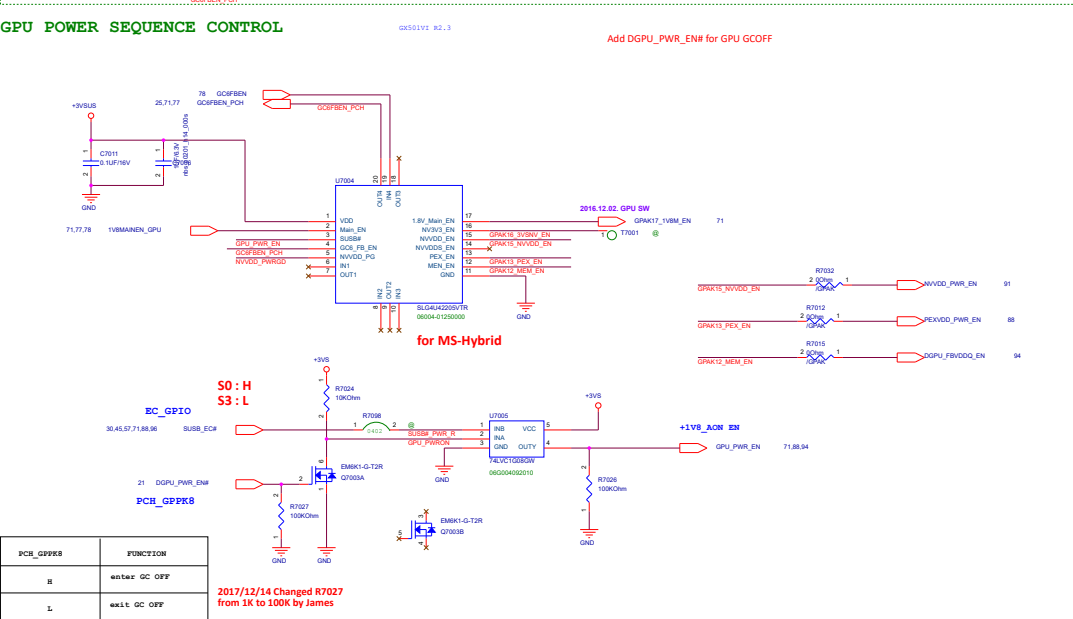
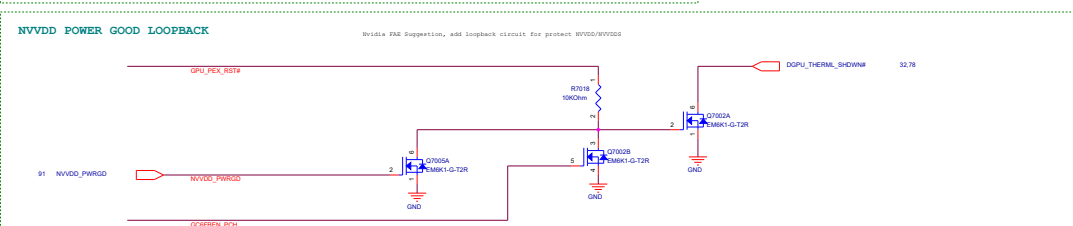
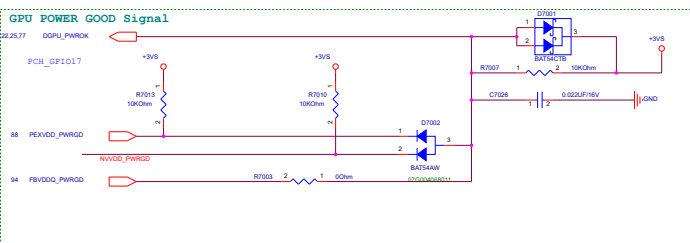


2016/07/27 EMI



<Core Design> 2017.05.02 EMI Reserve

ASUS		Title : OTH_EMI	
ASUSTek COMPUTER INC. NB1		Engineer: EE	
Size B	Project Name GX531GS	Rev 2.0	
Date: Thursday, July 19, 2018	Sheet	69	of 103



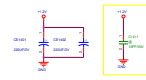
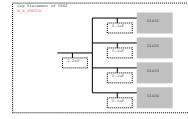
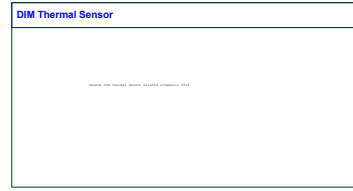
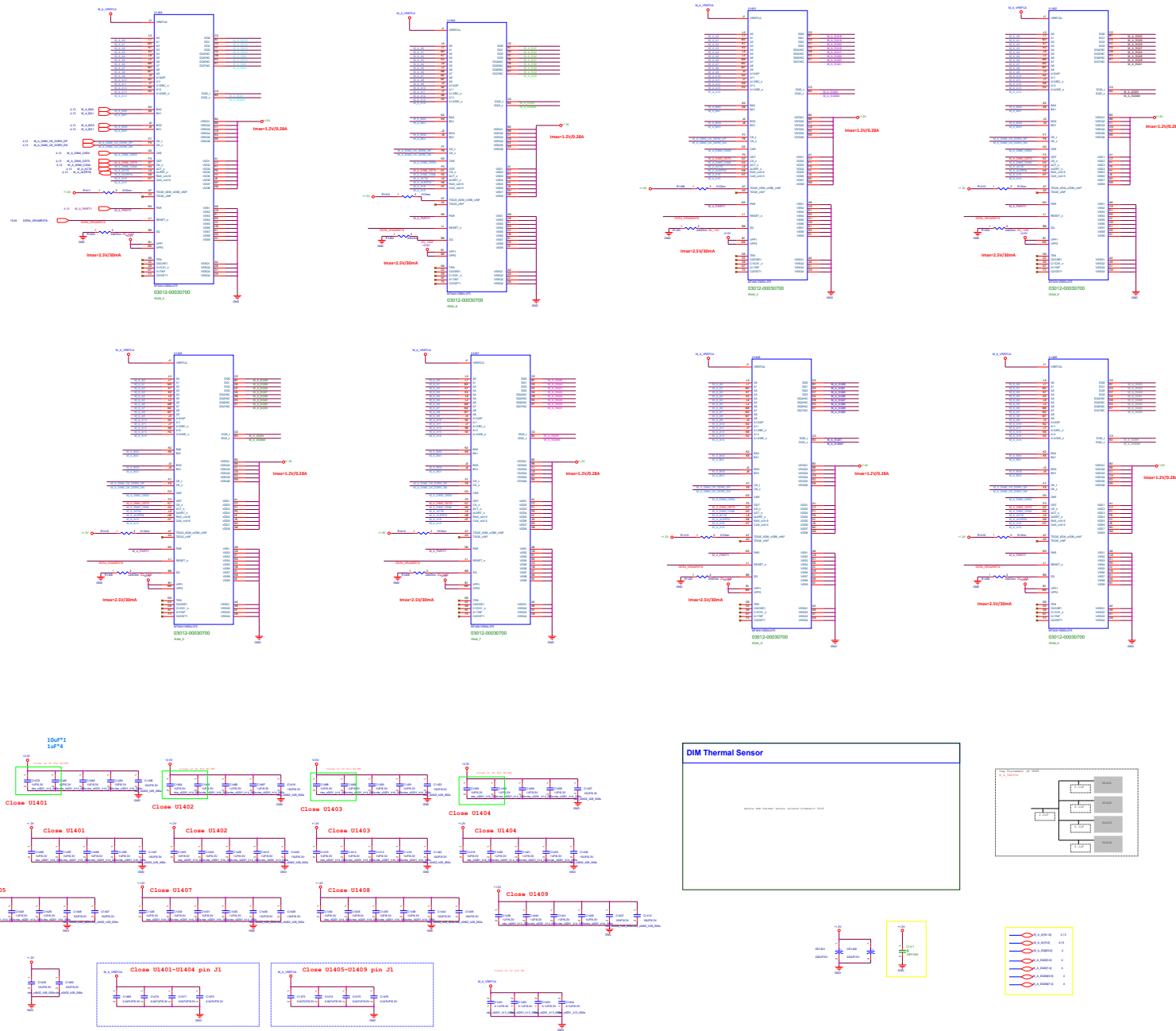
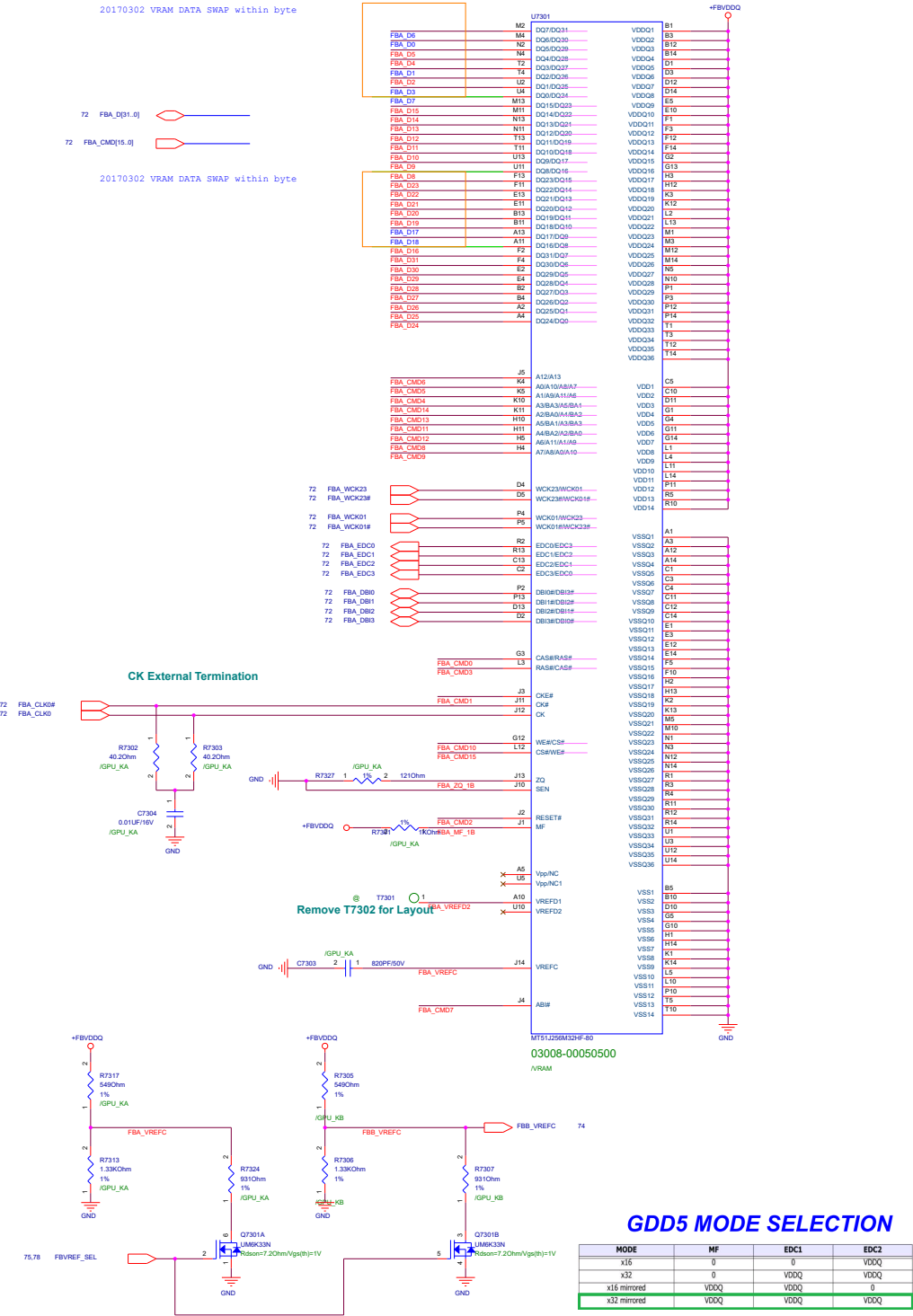


Table 4-35. DDR4 Memory Down Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x pF (size)	Note
DDR4 Memory Down x8-B Devices per Channel	VDDQ/VDD (shorted)	4 in row each x8 DRAM device as possible Distributed around the DRAM devices	4x4 1uF (0402) (min of 48 surface) 20x 10uF (0603) (min of 12 surface)	
	VTP	2 in row each x8 DRAM device as possible Distributed around the DRAM devices	32x 1uF (0402) 10x 10uF (0603)	
	VTT	Distributed along termination resistors	32x 1uF (0402)	
		Distributed evenly across domain	6x 10uF (0402)	

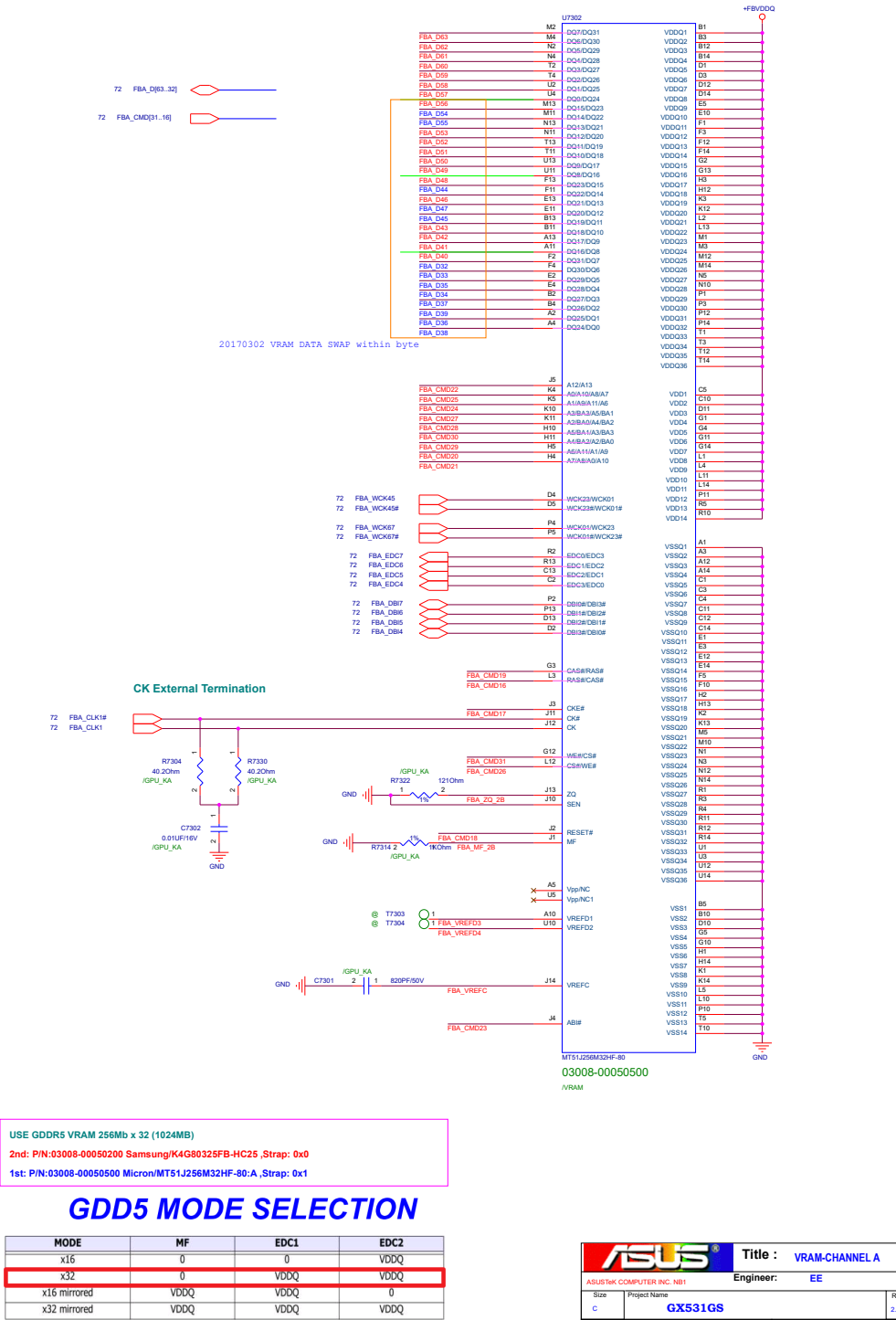
FBA Partition Memory (1 of 2)

MF=1 Mirror

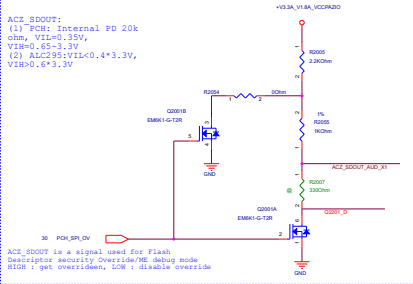
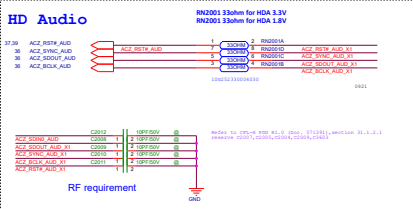


FBA Partition Memory (2 of 2)

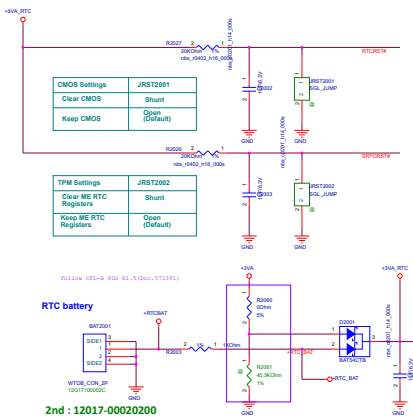
MF=0 Normal



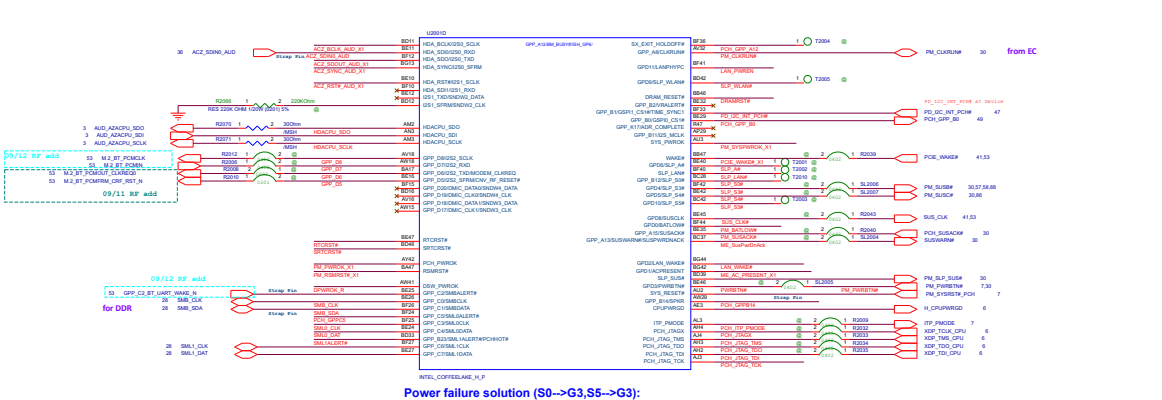
HD Audio



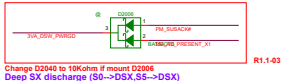
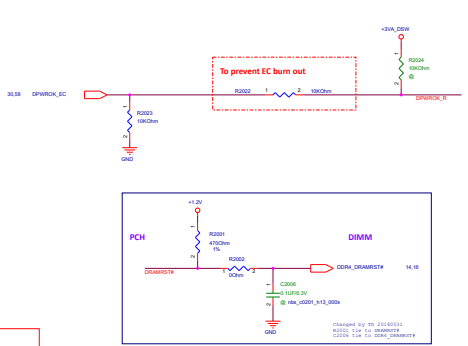
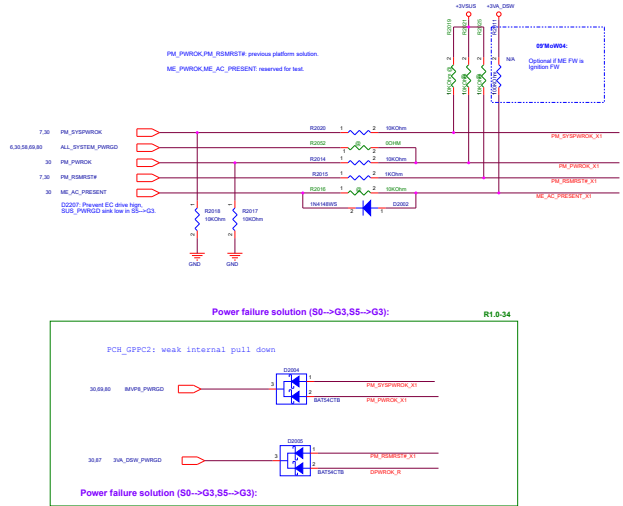
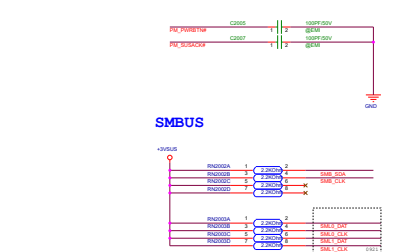
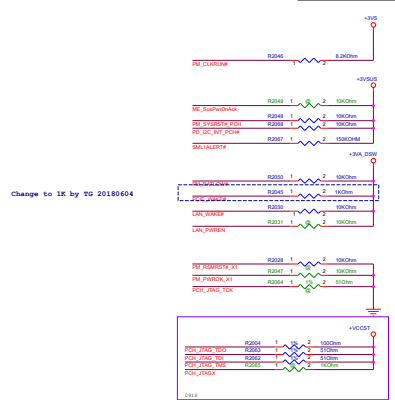
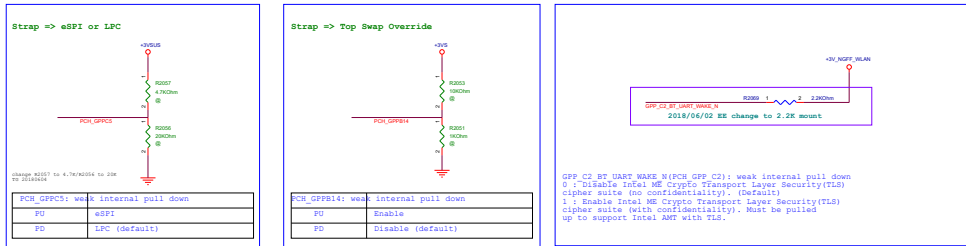
Main Source	1th PWR	2nd PWR	3rd PWR	4th
+RSTCBAT	+RSTC_BAT	+3VA_RTC		
AC_BAT_SYS	+1.05VSUS	+VCCST		
	+1.2V			
	+3VAG	+3VA	+3VA_EC	
	+3VA_DSN	+3VSUS	+3VSUS_PCH	+V2_3A_V1_5A_VCCM2
		+3VS		



USE RTC Battery:
P/N: 0B100-00040500 BATT-LI CR1220 3V



Power failure solution (S0-->G3,S5-->G3):



PCIE Setting

GX501G1 PCIE/SATA Function define

HSIO Capabilities	Function
PCIEG (From GPU)	
PCIE#01 - US83.1#07	
PCIE#02 - US83.1#08	
PCIE#03 - US83.1#09	
PCIE#04 - US83.1#10	
PCIE#05	
PCIE#06	
PCIE#07	
PCIE#08	
PCIE#09	PCIE9_SSD_P0
PCIE#10	PCIE10_SSD_P1
PCIE#11 - SATA-0a	PCIE11_SSD_P2/SATA
PCIE#12 - SATA-1a	PCIE12_SSD_P3/SATA
PCIE#13 - SATA-0b	
PCIE#14 - SATA-1b	
PCIE#15 / SATA#2	
PCIE#16 / SATA#3	WLAN
PCIE#17 / SATA#4	
PCIE#18 / SATA#5	
PCIE#19 / SATA#6	
PCIE#21	
PCIE#22	
PCIE#23	
PCIE#24	

CLKREQ-0	GPU
CLKREQ-1	
CLKREQ-2	WLAN
CLKREQ-3	
CLKREQ-4	
CLKREQ-5	
CLKREQ-6	SSD CPU
CLKREQ-7	
CLKREQ-8	
CLKREQ-9	
CLKREQ-10~15	

USB Setting

GX501G1 USB Function define

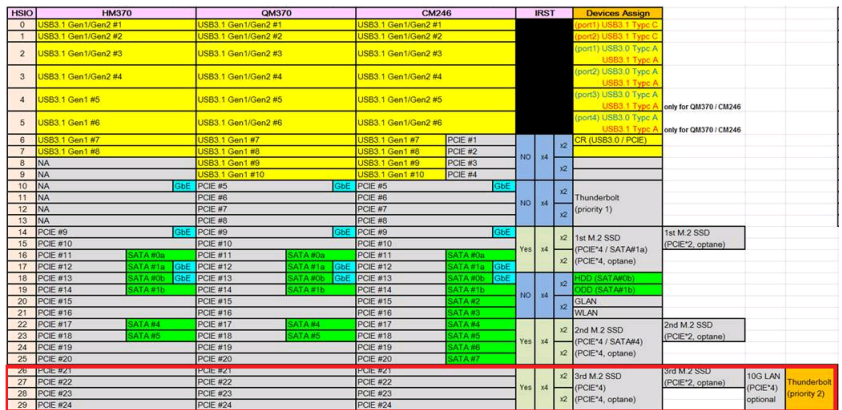
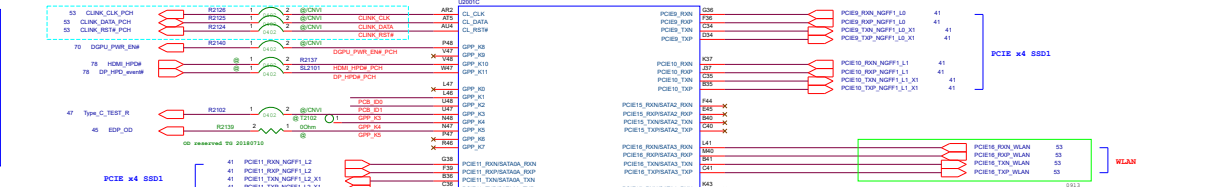
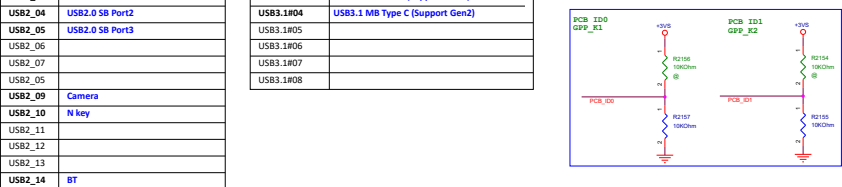
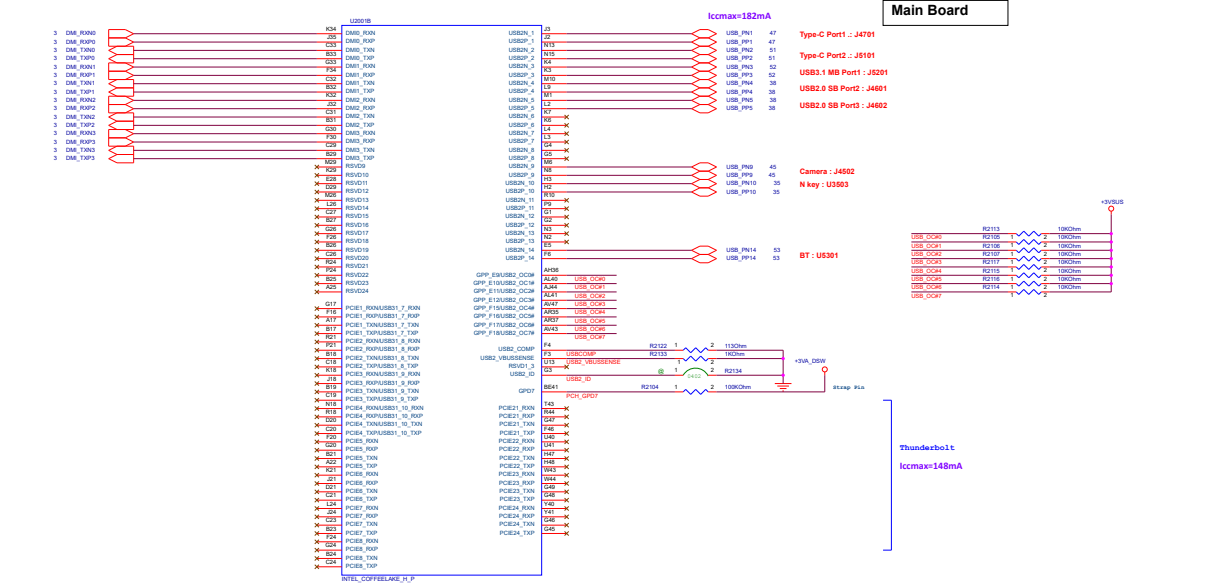
USB 2.0	Function
US82_01	US83.1 Type C
US82_02	US83.1 Type C
US82_03	US83.1 MB Port1
US82_04	US82.0 SB Port2
US82_05	US82.0 SB Port3
US82_06	
US82_07	
US82_08	Camera
US82_10	N key
US82_11	
US82_12	
US82_13	
US82_14	BT

CNL

HM370

USB 3.0	Function
US83.1#01	US83.1 MB Type C (Support Gen2)
US83.1#02	US83.1 MB Type C (Support Gen2)
US83.1#03	US83.1 MB Port3 (Support Gen2)
US83.1#04	US83.1 MB Type C (Support Gen2)
US83.1#05	
US83.1#06	
US83.1#07	
US83.1#08	

HSIO	HM370	QM370	CM246	IRST	Devices Assign
1	US83.1 Gen1/Gen2 #1	US83.1 Gen1/Gen2 #1	US83.1 Gen1/Gen2 #1	0	(port0) US83.1 Type C
2	US83.1 Gen1/Gen2 #2	US83.1 Gen1/Gen2 #2	US83.1 Gen1/Gen2 #2	0	(port2) US83.1 Type C
3	US83.1 Gen1/Gen2 #3	US83.1 Gen1/Gen2 #3	US83.1 Gen1/Gen2 #3	0	(port1) US83.0 Type A
4	US83.1 Gen1/Gen2 #4	US83.1 Gen1/Gen2 #4	US83.1 Gen1/Gen2 #4	0	(port0) US83.1 Type A
5	US83.1 Gen1 #5	US83.1 Gen1/Gen2 #5	US83.1 Gen1/Gen2 #5	0	(port3) US83.0 Type A
6	US83.1 Gen1 #6	US83.1 Gen1/Gen2 #6	US83.1 Gen1/Gen2 #6	0	(port4) US83.1 Type A
7	US83.1 Gen1 #7	US83.1 Gen1 #7	US83.1 Gen1 #7	0	CR (US83.0 / PCIE)
8	US83.1 Gen1 #8	US83.1 Gen1 #8	US83.1 Gen1 #8	0	PCIE #1
9	US83.1 Gen1 #9	US83.1 Gen1 #9	US83.1 Gen1 #9	0	PCIE #2
10	US83.1 Gen1 #10	US83.1 Gen1 #10	US83.1 Gen1 #10	0	PCIE #3
11	US83.1 Gen1 #11	US83.1 Gen1 #11	US83.1 Gen1 #11	0	PCIE #4
12	US83.1 Gen1 #12	US83.1 Gen1 #12	US83.1 Gen1 #12	0	PCIE #5
13	US83.1 Gen1 #13	US83.1 Gen1 #13	US83.1 Gen1 #13	0	PCIE #6
14	US83.1 Gen1 #14	US83.1 Gen1 #14	US83.1 Gen1 #14	0	PCIE #7
15	US83.1 Gen1 #15	US83.1 Gen1 #15	US83.1 Gen1 #15	0	PCIE #8
16	US83.1 Gen1 #16	US83.1 Gen1 #16	US83.1 Gen1 #16	0	PCIE #9
17	US83.1 Gen1 #17	US83.1 Gen1 #17	US83.1 Gen1 #17	0	PCIE #10
18	US83.1 Gen1 #18	US83.1 Gen1 #18	US83.1 Gen1 #18	0	PCIE #11
19	US83.1 Gen1 #19	US83.1 Gen1 #19	US83.1 Gen1 #19	0	PCIE #12
20	US83.1 Gen1 #20	US83.1 Gen1 #20	US83.1 Gen1 #20	0	PCIE #13
21	US83.1 Gen1 #21	US83.1 Gen1 #21	US83.1 Gen1 #21	0	PCIE #14
22	US83.1 Gen1 #22	US83.1 Gen1 #22	US83.1 Gen1 #22	0	PCIE #15
23	US83.1 Gen1 #23	US83.1 Gen1 #23	US83.1 Gen1 #23	0	PCIE #16
24	US83.1 Gen1 #24	US83.1 Gen1 #24	US83.1 Gen1 #24	0	PCIE #17
25	US83.1 Gen1 #25	US83.1 Gen1 #25	US83.1 Gen1 #25	0	PCIE #18
26	US83.1 Gen1 #26	US83.1 Gen1 #26	US83.1 Gen1 #26	0	PCIE #19
27	US83.1 Gen1 #27	US83.1 Gen1 #27	US83.1 Gen1 #27	0	PCIE #20
28	US83.1 Gen1 #28	US83.1 Gen1 #28	US83.1 Gen1 #28	0	PCIE #21
29	US83.1 Gen1 #29	US83.1 Gen1 #29	US83.1 Gen1 #29	0	PCIE #22
30	US83.1 Gen1 #30	US83.1 Gen1 #30	US83.1 Gen1 #30	0	PCIE #23
31	US83.1 Gen1 #31	US83.1 Gen1 #31	US83.1 Gen1 #31	0	PCIE #24

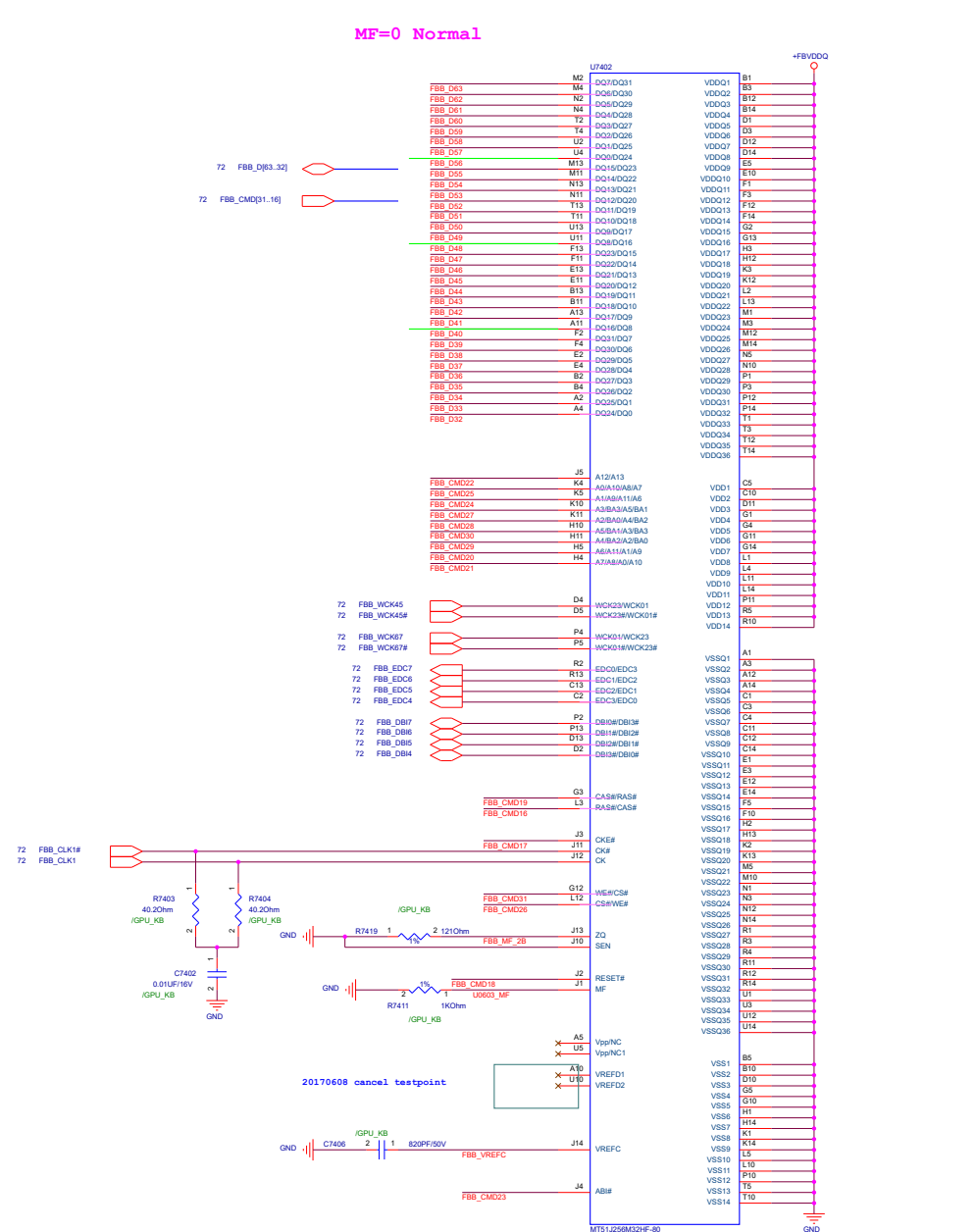
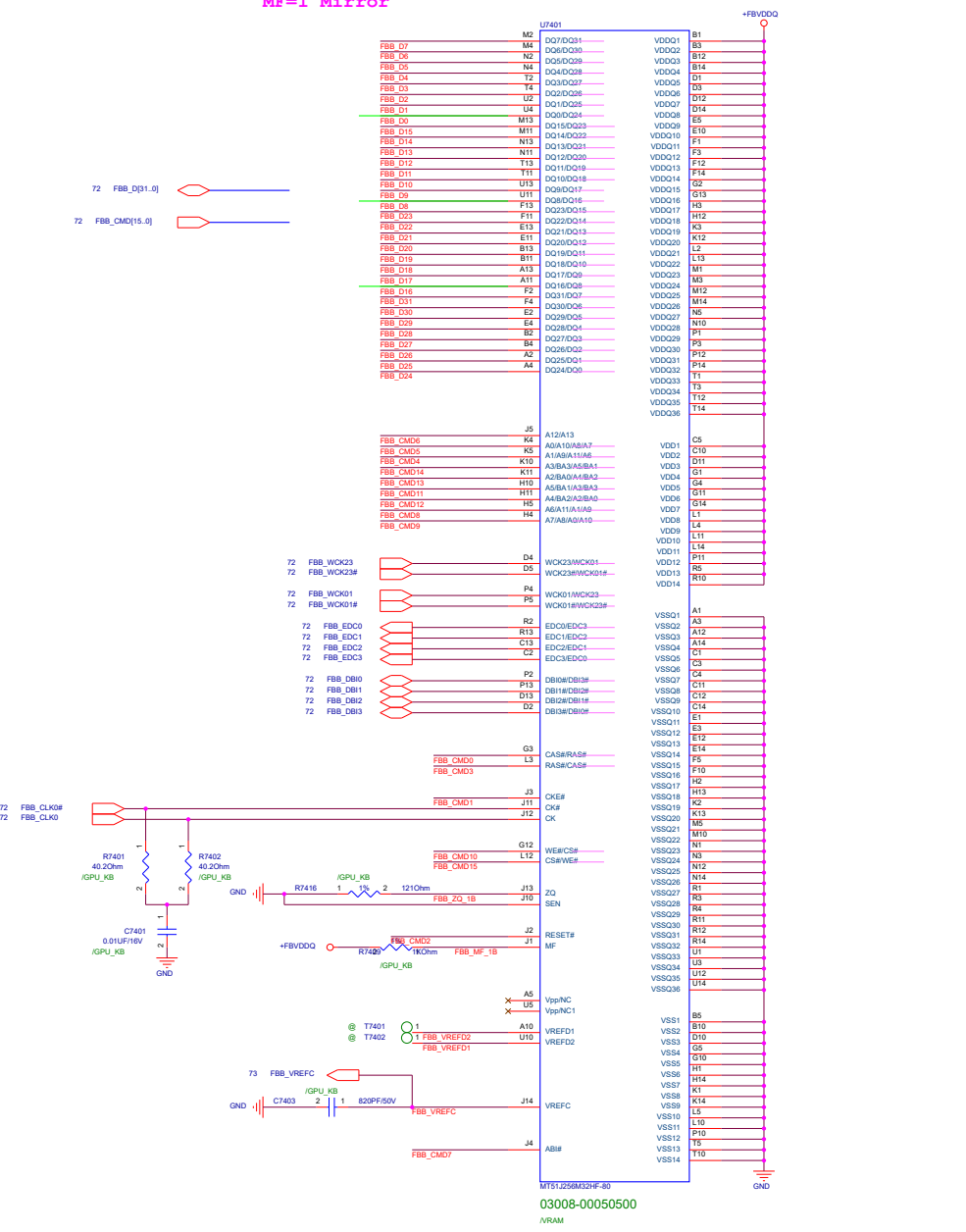


FBB Partition Memory (1 of 2)

FBB Partition Memory (2 of 2)

MF=1 Mirror

MF=0 Normal



USE GDDR5 VRAM 256Mb x 32 (1024MB)
1st: P/N:03008-00050200 Samsung/K4G80325FB-HC25, Strap: 0x0
2nd: P/N:03008-00050500 Micron/MT51J256M32HF-80 A, Strap: 0x1

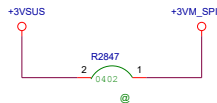
GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

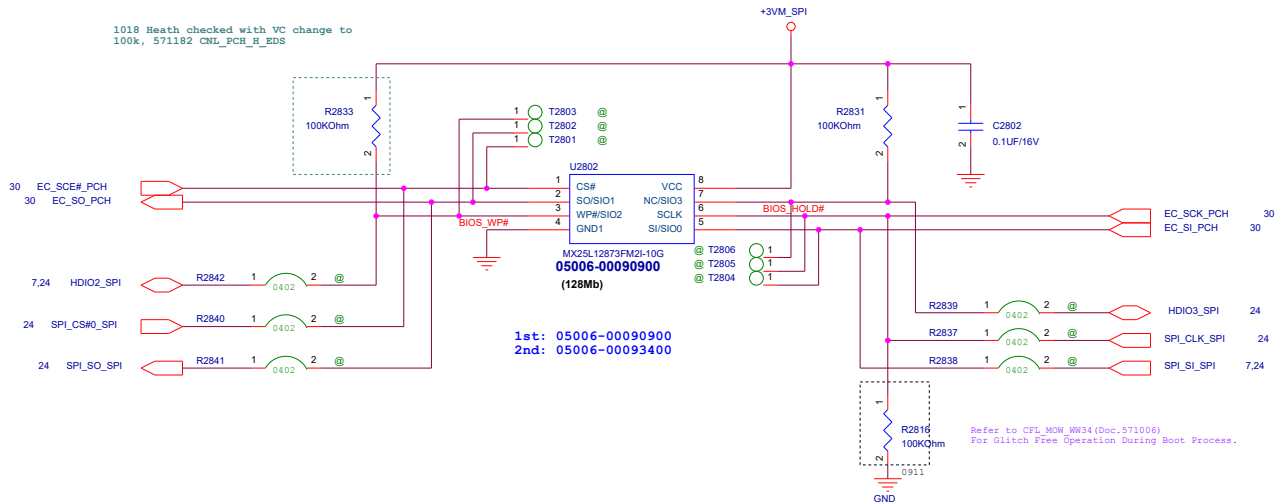
SPI Power



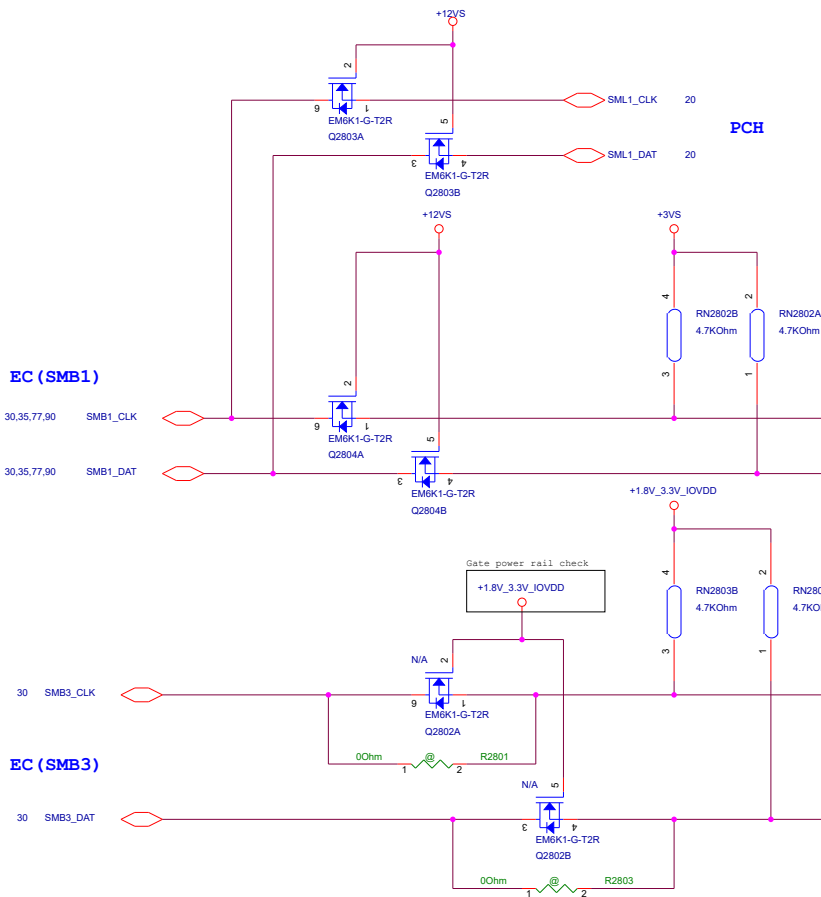
1st SPI ROM

1st: 05006-00090900 FLASH MXIC MX25L12873FM2I-10G 128M SOP-8L

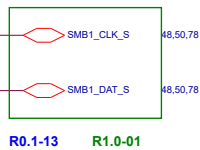
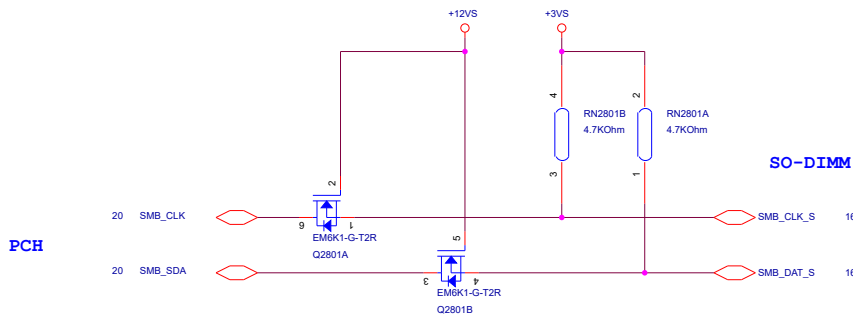
2nd: 05006-00093100 FLASH GD25B127DSIGG IGDADEVICE 128MB SOP8



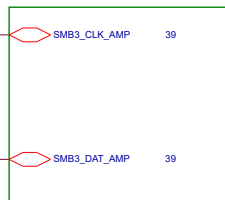
System Management Interface



SMBus Interface



CPU, VGA Thermal Sensor
Power Thermal Sensor

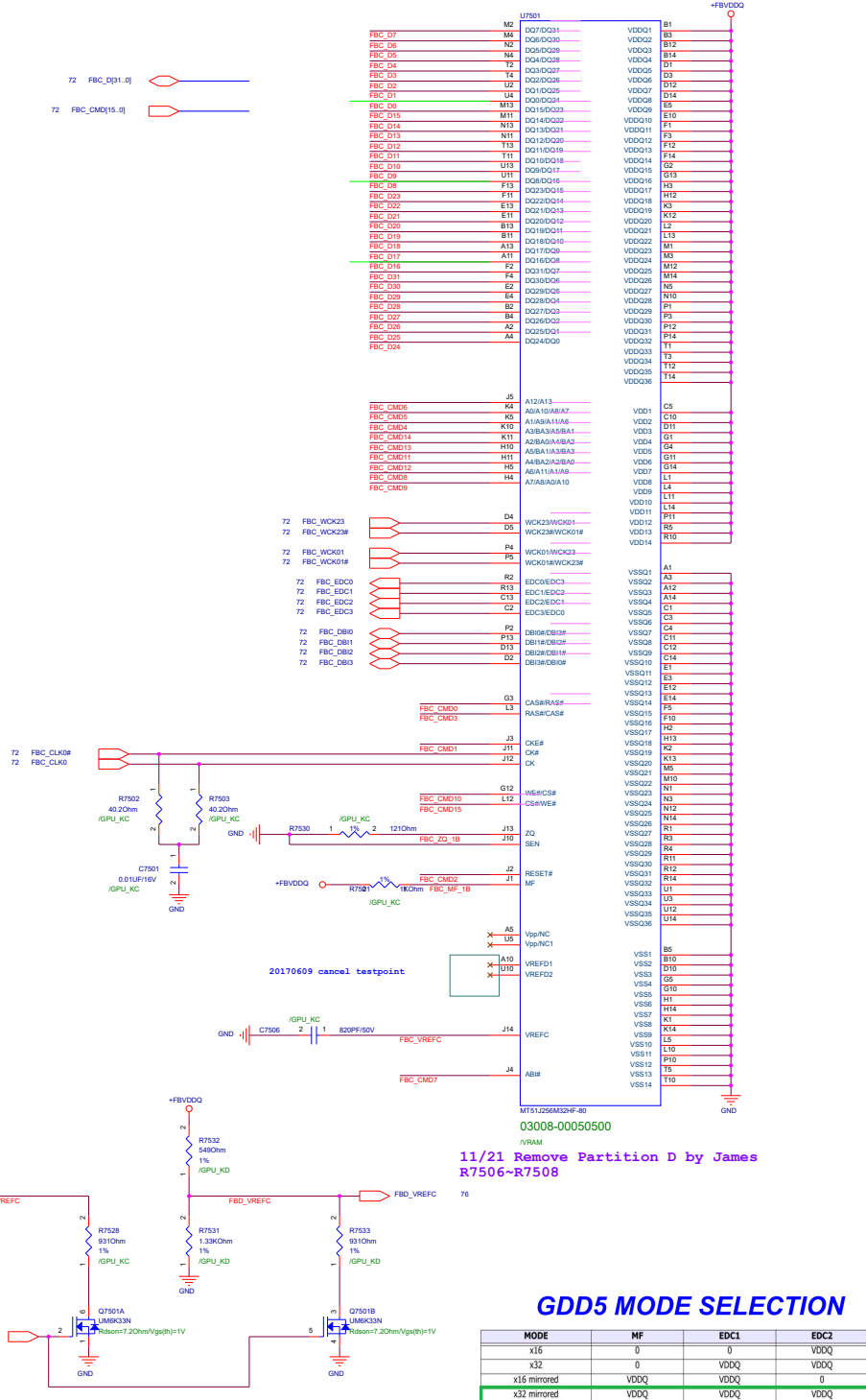


GX501VI R1,1 for smart amp

ASUS		Project Name	Rev
GX531GS			2.0
Title : PCH-SPI ROM, OTH			
Size	Dept.:	ASUSTek COMPUTER	Engineer: EE
Custom	Date: Thursday, July 19, 2018	Sheet	28 of 103

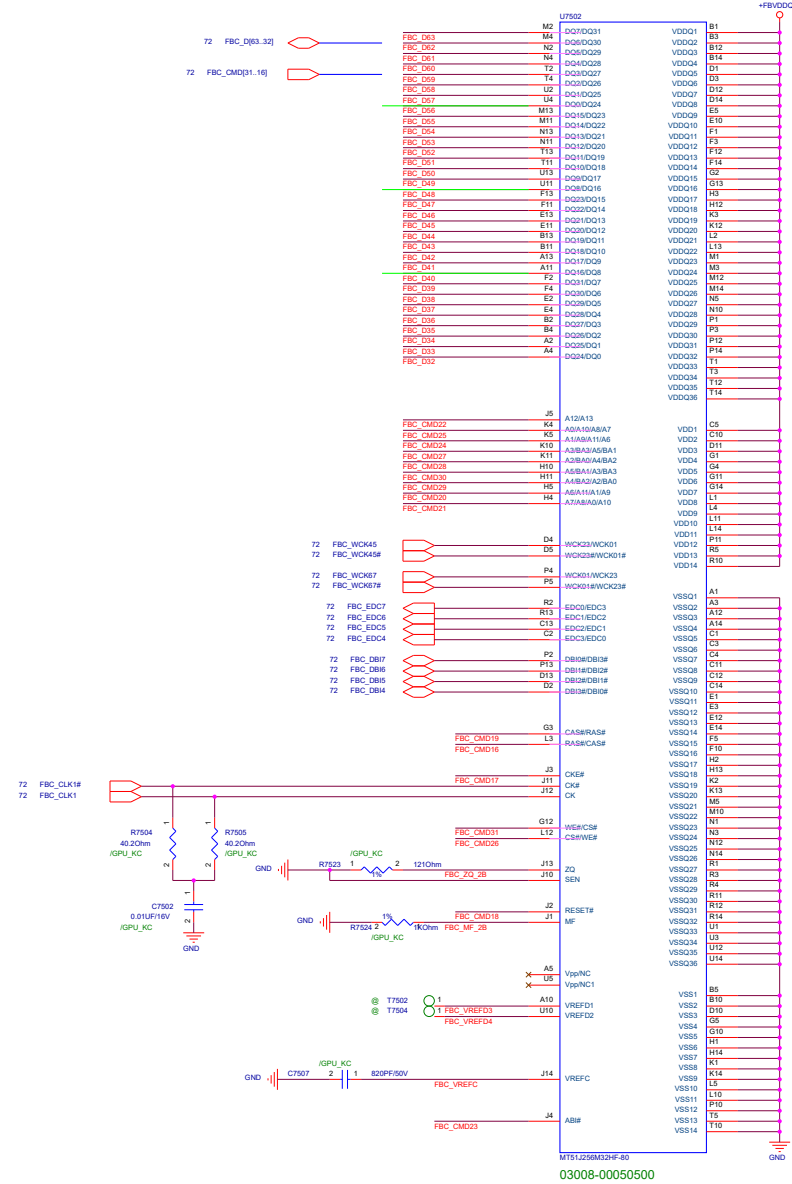
FBC Partition Memory (1 of 2)

MF=1 Mirror



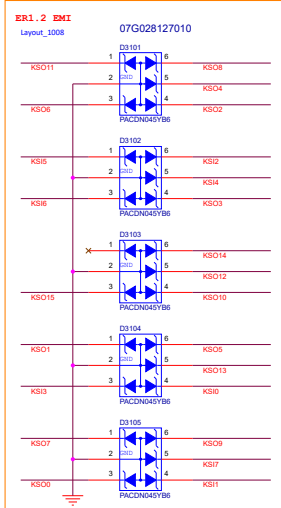
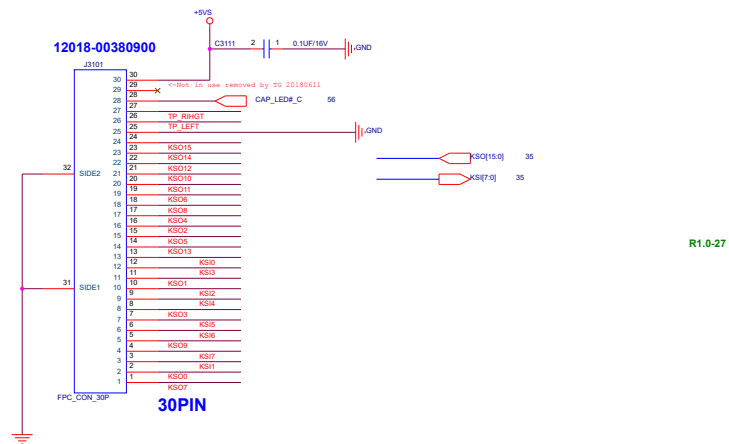
FBC Partition Memory (2 of 2)

MF=0 Normal



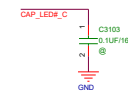
GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ

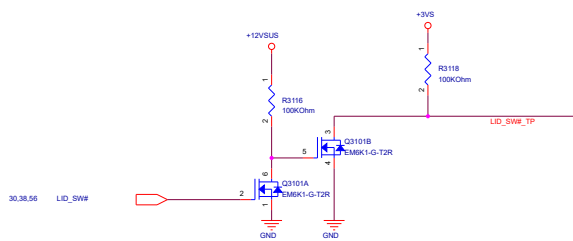
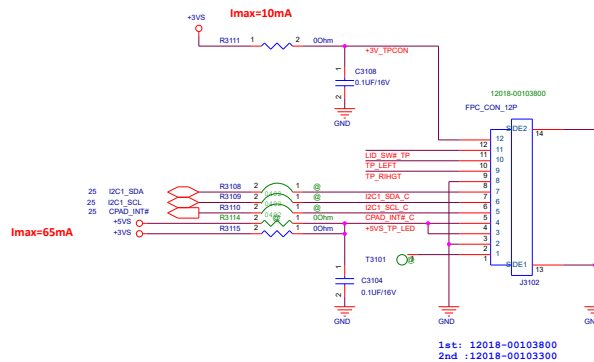


R1.1-4/13-5

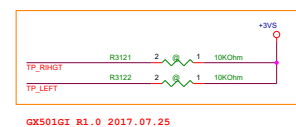
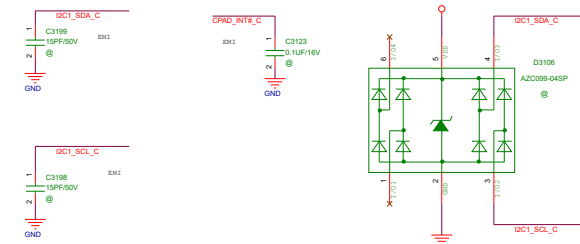
D3102-D317 ESD PROTECTION AE2115-05C
1st Source: P/N:07G028162010 NXP SOT363
2nd Source: P/N:07G028127010 AMAZING SC70-6L



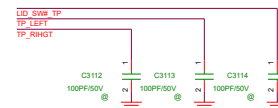
Touch Pad / Ten Keys Connector



Reserved for EMI



GX501GI R1.0 2017.07.25



2018/01/04 for EMI Reserved

Touch Pad Pin Define

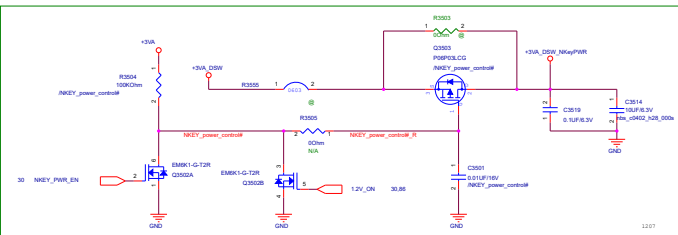
Connector type: 12 pins FFC connector, pitch is 0.5 mm.

Pin		Signal	CN1 pin assignment and description	Description
1	VDD_3.3V		Power	3.3V +/-5%. Power supply: 100 mV/pp max. Power sequence: See section 4.6.
2	LID_CLOSE	I		Lid close/open pin. Indicates that the lid is closed or opened. Low when lid is closed. High when lid is opened.
3	SWL	I		Low active, left button signal.
4	SWR	I		Low active, right button signal.
5	GND	GND		Ground
6	SDA	I/O		I ² C data. I/Os of I/Os: 8 mA max.
7	SCL	I/O		I ² C clock. I/Os of I/Os: 8 mA max.
8	INT	O		Active low, indicates that the touchpad wants to send data to host
9	LED_VDD		Power	Power for LED circuit. 3.3V, driver current: TBD

10	LED_VDD	Power	Power for LED circuit. 3.3V; driver current: TBD
11	GND	GND	Ground
12	LED_CONTROL	I	To lighten the LED when high. High active

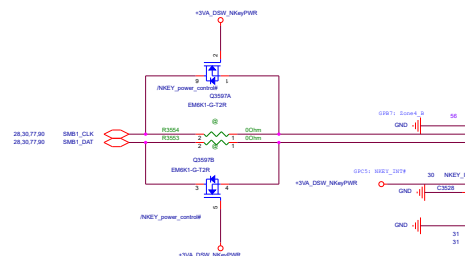
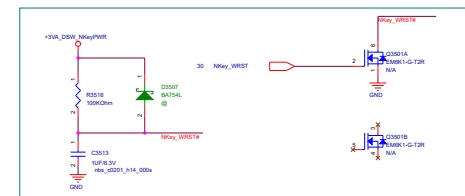
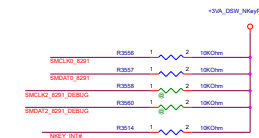
<Core Design>

For EC Reset N_key

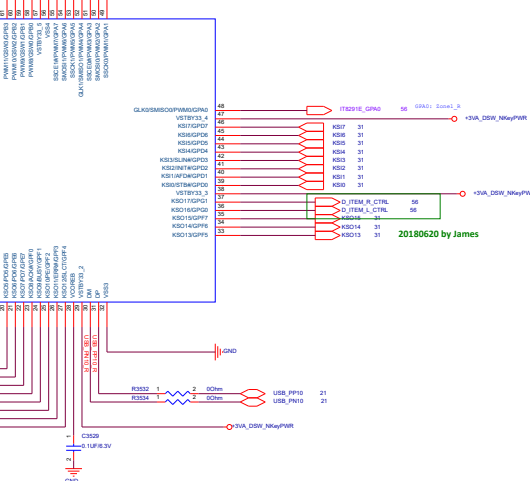
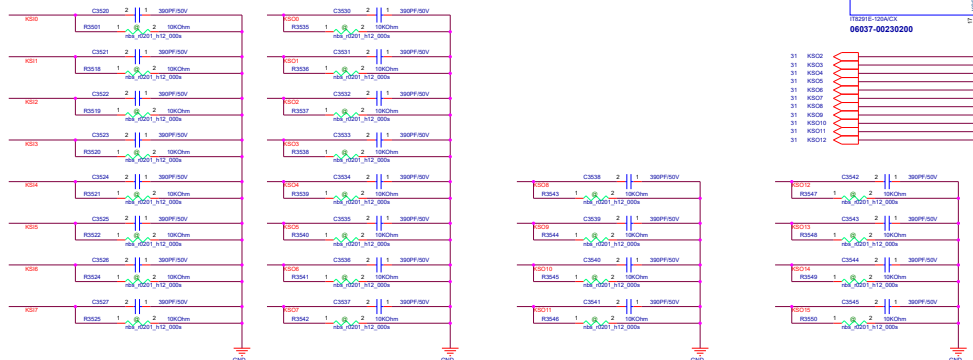


S5-: before shutdown special effects finish
S5: after shutdown special effects finish

S5-: before shutdown special effects finish
S5: after shutdown special effects finish



For ESD



GPI0	Net name	GPI0	Net name
GPA0	Zone1_R	GPB0	Zone2_G
GPA1	Zone1_G	GPB1	Zone2_B
GPA2	Zone1_B	GPB2	Zone3_R
GPA3	Zone2_R	GPB3	Zone3_G
GPA4	PWR_LED	GPB4	Zone3_B
GPA5	D_item_R	GPB5	Zone4_R
GPA6	D_item_G	GPB6	Zone4_G
GPA7	D_item_B	GPB7	Zone4_B

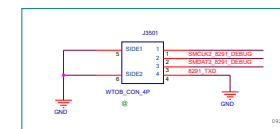
For DS3 wake from KB

Use NEY-INT# to substitute
0920

For S4/S5 don't wake from KB

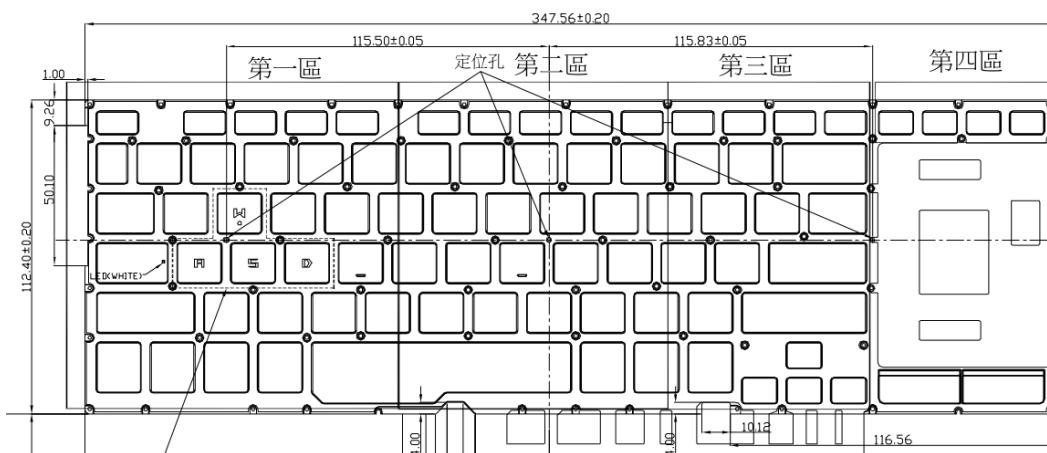
Use NEY-INT# to substitute
0920

ITE 8291 debug con



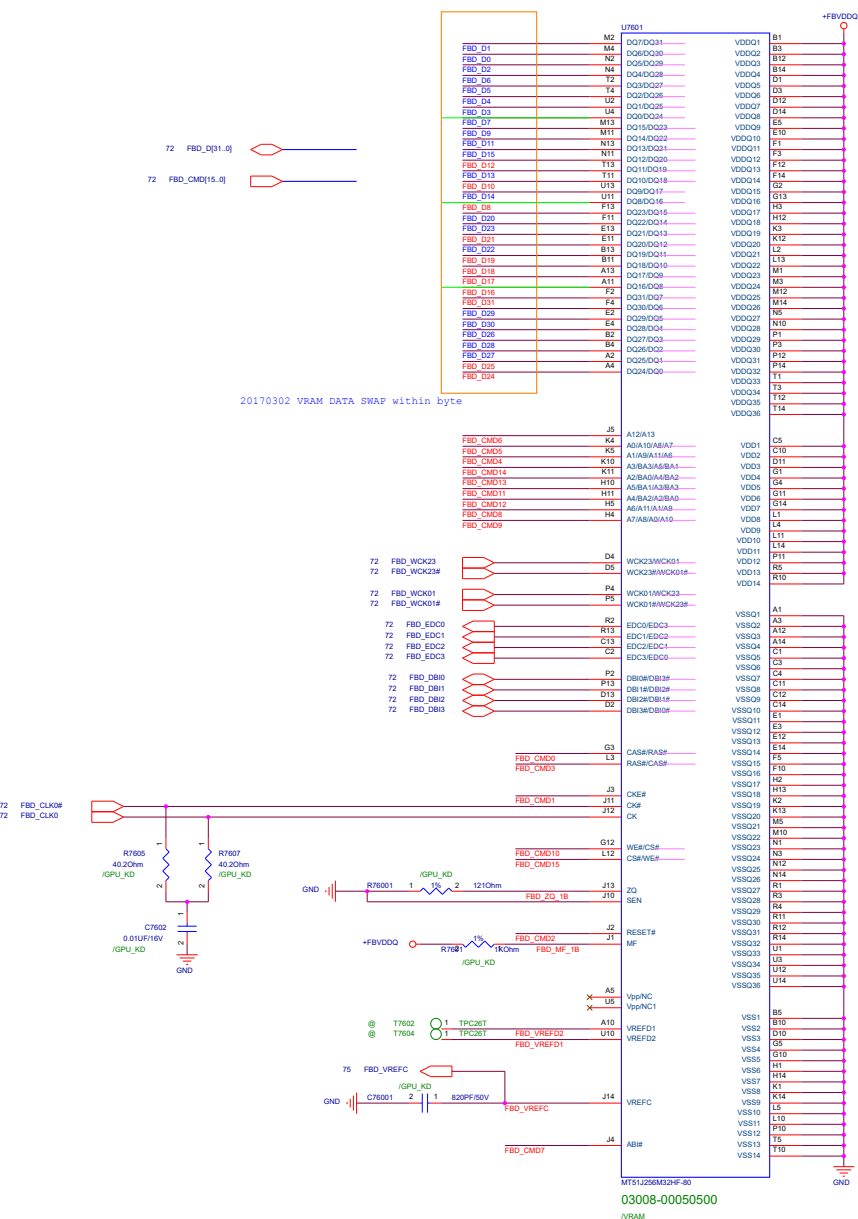
GX501GI- SR Stuff

Keryboard sepc and N-key GPIO compare



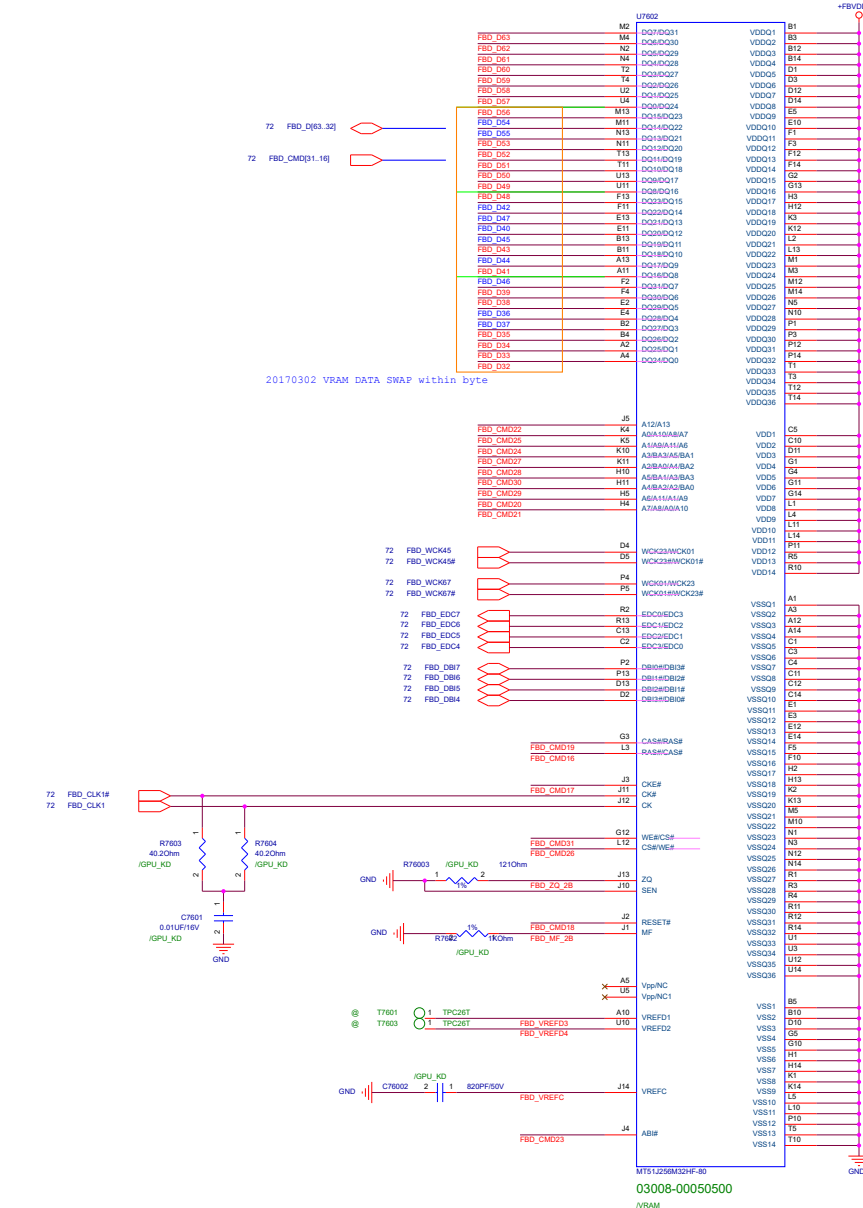
FBD Partition Memory (1 of 2)

MF=1 Mirror



FBD Partition Memory (2 of 2)

MF=0 Normal



R1.3-02 R1.2-25

USE GDDR5 VRAM 128Mb x 32 (512MB)

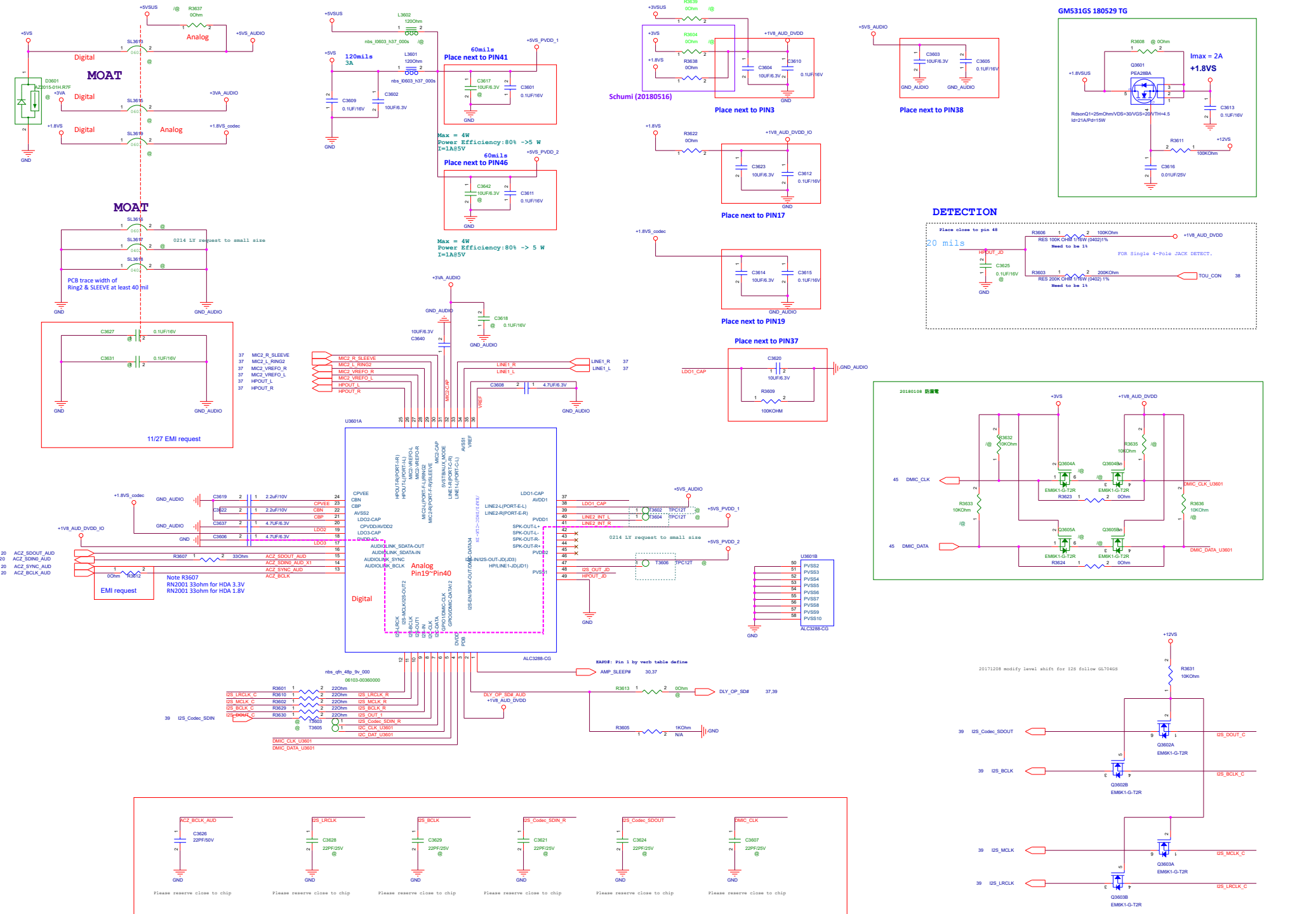
1st: P/N:03008-00030100 HYNIX/H5GC4H24MFR-T2C (M-die) ,Strap: 0x2

2nd: P/N:03008-00030200 SAMSUNG/K4G41325FC-HC03 ,Strap: 0x3

3rd: P/N:03008-00030400 Micron/EDW4032BABG-60-F (B-die) ,Strap: 0x4

GDD5 MODE SELECTION

MODE	MF	EDC1	EDC2
x16	0	0	VDDQ
x32	0	VDDQ	VDDQ
x16 mirrored	VDDQ	VDDQ	0
x32 mirrored	VDDQ	VDDQ	VDDQ



0221 change to 0201 for LY routing

<Core Design

Project Name		Rev
ASUS		
Title : AUD ALC3288-CG		
Size	Dept.: ASUSÜtÜk COMPUTER INC.	Engineer: EE
Date: Thursday, July 19, 2016	Sheet	36 of 102

R1.2
RESET# should keep high when loading the initial code[Prevent pull low from EC]

Max = 4W / Channel
I = 0.7 A (@Speaker : 8 Ohm)

SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 40 mils

INTERNAL SPK Conn.

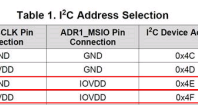
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 30mils

Check pin define

2nd: 12G17000004V

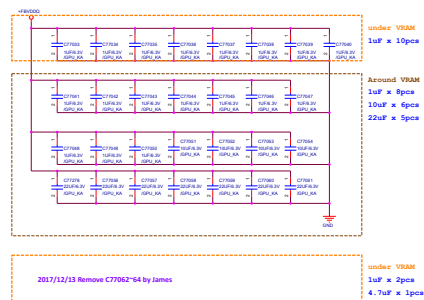
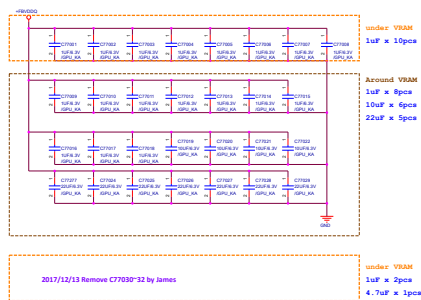
SPK L+ L- R+ R- trace width
Speaker 4 ohm ==> 60mils

- **Boost Input (terminal: VBAT)**
 - Voltage: 2.9 V to 5.5 V
 - Max Current: 5 A for ILIM = 3.0 A (default)
- **Analog Supply (terminal: AVDD)**
 - Voltage: 1.65 V to 1.95 V
 - Max Current: 30 mA
- **Digital Supply (terminal: DVDD)**
 - Voltage: 1.65 V to 1.95 V
 - Max Current: TBD mA
- **Digital I/O Supply (terminal: IOVDD)**
 - Voltage: 1.62 V to 3.6 V
 - Max Current: 5 mA

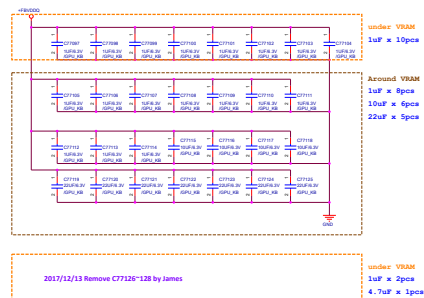
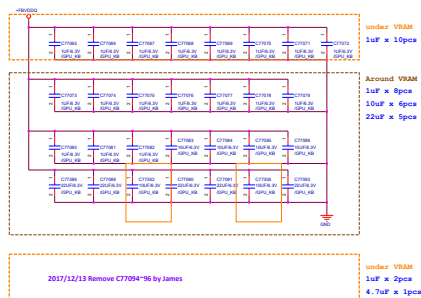


ADR0_SCLK Pin Connection	ADR1_MSIO Pin Connection	I ² C Device Address
GND	GND	0x4C
IOVDD	GND	0x4D
GND	IOVDD	0x4E
IOVDD	IOVDD	0x4F

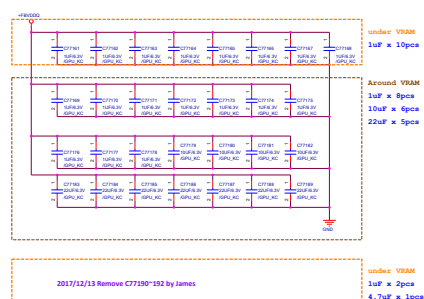
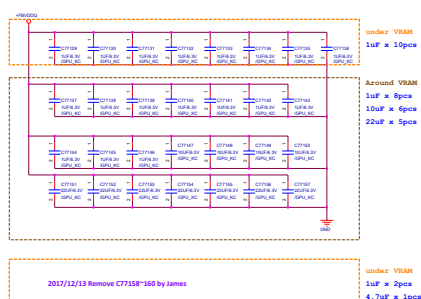
Channel A



Channel B

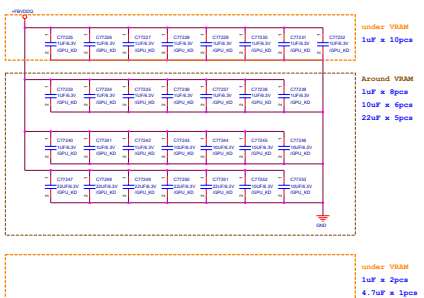
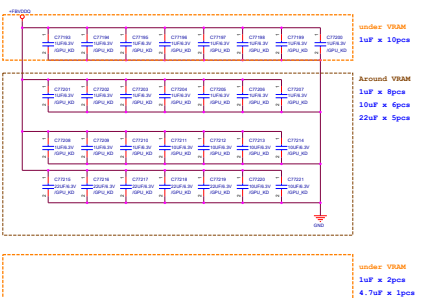


Channel C



Channel D

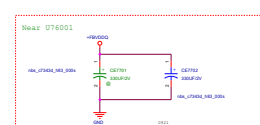
11/21 Remove Partition D Caps by James
C77183-C77224/C77225-C77256



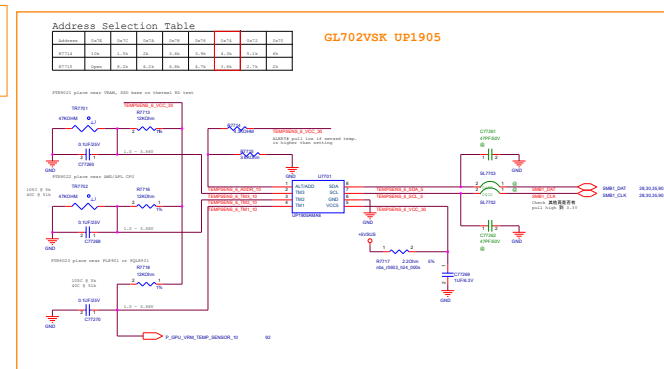
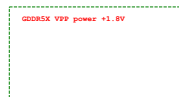
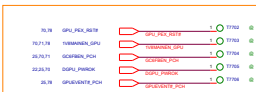
Del C77222, C77223, C77224 due to GD805 didn't need VPP
River 6/23

Del C77224, C77225, C77226 due to GD805 didn't need VPP
River 6/23

VRAM PWR_FBDDQ



For power sequence measurement



R _{ds(on)}	Min. Current Load (mA)	Typ. Current Load (mA)	Max. Current Load (mA)
6.5k	2700	3000	3300
7.6k	2400	2700	2970
8.25k	2250	2550	2775
9.53k	1980	2250	2430
10.5k	1800	2000	2200
11.5k	1620	1800	1980
14.3k	1350	1500	1650
17.4k	1080	1250	1320
21k	900	1050	1100

Panel Vender : AUO
PN : B156HAN08.2(HW 2A)

PIN NO	Symbol	PIN NO	Symbol
1	NC	24	LCD GND
2	NC	25	LCD GND
3	ane3_N	26	LCD GND
4	ane3_P	27	HFD
5	H_GND	28	BL GND
6	ane2_N	29	BL GND
7	ane2_P	30	BL GND
8	H_GND	31	BL GND
9	ane1_N	32	BL Enable
10	ane1_P	33	BL PWM DA
11	H_GND	34	NC
12	ane0_N	35	NC
13	ane0_P	36	BL PWR
14	BL_GND	37	BL PWR
15	AUX1_CH1_P	38	BL PWR
16	AUX1_CH1_N	39	BL PWR
17	NC	40	NC
18	LCD_VCC		
19	LCD_VCC		
20	LCD_VCC		
21	LCD_VCC		
22	CSD_50%_test		
23	NC		

Reserved for '+3V3_LDO' design ID 20180607

Figure 1 shows 23 DNA constructs. Each construct is represented by a horizontal line with various features labeled. The constructs are numbered 1 through 23. The features include:

- CMV**: CMV promoter (red line)
- MCS**: Multiple cloning site (blue line)
- GFP**: Green fluorescent protein gene (green line)
- EGFP**: Enhanced green fluorescent protein gene (green line)
- EGFP-X1**: EGFP gene with a specific mutation (green line)
- EGFP-X2**: EGFP gene with a specific mutation (green line)
- EGFP-X3**: EGFP gene with a specific mutation (green line)
- EGFP-X4**: EGFP gene with a specific mutation (green line)
- EGFP-X5**: EGFP gene with a specific mutation (green line)
- EGFP-X6**: EGFP gene with a specific mutation (green line)
- EGFP-X7**: EGFP gene with a specific mutation (green line)
- EGFP-X8**: EGFP gene with a specific mutation (green line)
- EGFP-X9**: EGFP gene with a specific mutation (green line)
- EGFP-X10**: EGFP gene with a specific mutation (green line)
- EGFP-X11**: EGFP gene with a specific mutation (green line)
- EGFP-X12**: EGFP gene with a specific mutation (green line)
- EGFP-X13**: EGFP gene with a specific mutation (green line)
- EGFP-X14**: EGFP gene with a specific mutation (green line)
- EGFP-X15**: EGFP gene with a specific mutation (green line)
- EGFP-X16**: EGFP gene with a specific mutation (green line)
- EGFP-X17**: EGFP gene with a specific mutation (green line)
- EGFP-X18**: EGFP gene with a specific mutation (green line)
- EGFP-X19**: EGFP gene with a specific mutation (green line)
- EGFP-X20**: EGFP gene with a specific mutation (green line)
- EGFP-X21**: EGFP gene with a specific mutation (green line)
- EGFP-X22**: EGFP gene with a specific mutation (green line)
- EGFP-X23**: EGFP gene with a specific mutation (green line)

[illegible]

Figure 1 shows four schematic diagrams of 1T1R1C1 memristor-based crossbar arrays. Each diagram consists of a central white square representing the array, with red lines for word lines and blue lines for bit lines. The arrays are labeled (a) through (d). Each array has a word line labeled 'W' and a bit line labeled 'B'. The arrays are connected to word lines and bit lines via access transistors (AT) and memristors (M). The arrays are labeled with their respective word line and bit line labels: (a) W1, B1, (b) W2, B2, (c) W3, B3, and (d) W4, B4. The arrays are connected to word lines and bit lines via access transistors (AT) and memristors (M). The arrays are labeled with their respective word line and bit line labels: (a) W1, B1, (b) W2, B2, (c) W3, B3, and (d) W4, B4.

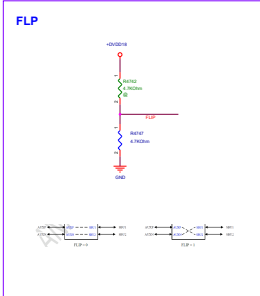
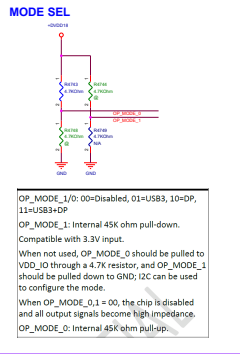
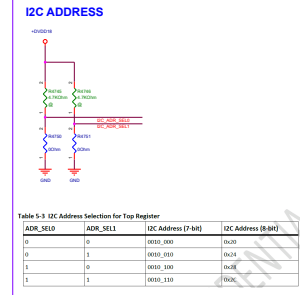
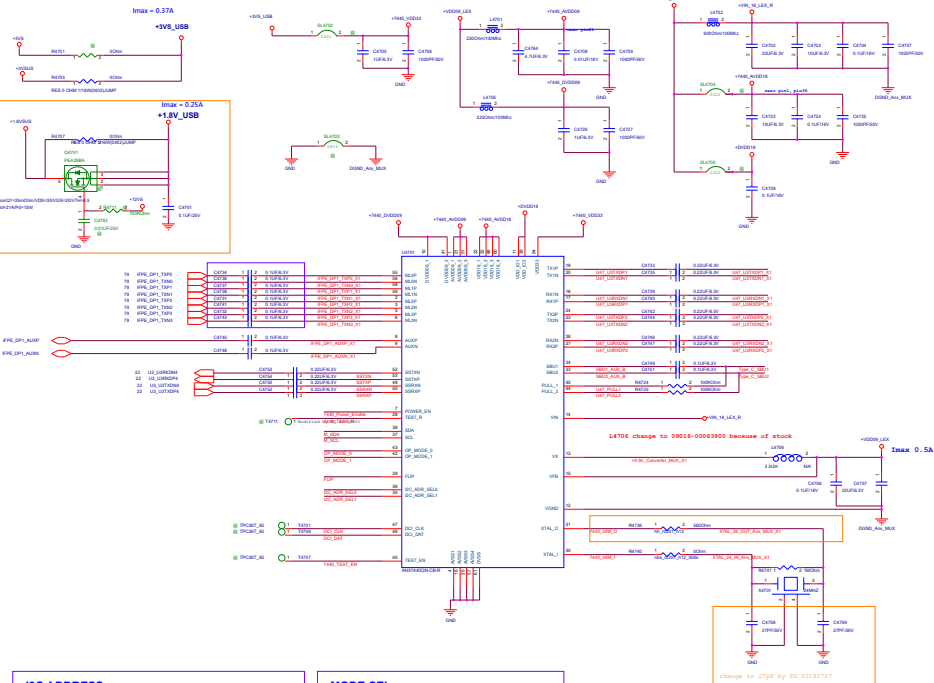
Normal : L (OD disable)
Active : H (OD enable)

EXP_HPRD_CONN

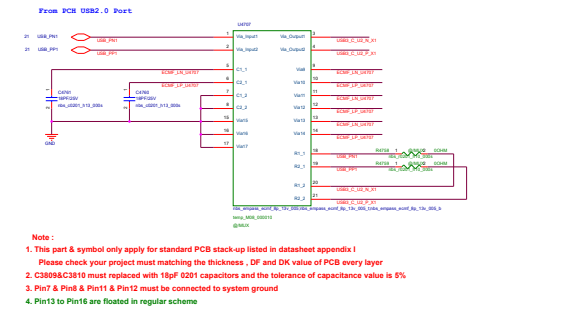
[illegible][illegible]

The figure contains two circuit diagrams. The left diagram is a full-bridge inverter with two legs. Each leg consists of a MOSFET (Q1, Q2) and a diode (D1, D2) in series. The MOSFETs are driven by a PWM signal (PWM) and a complementary signal (PWMN). The diodes are connected to ground. The load inductor (L) is connected between the two MOSFETs. The right diagram is a half-bridge inverter with one leg. It consists of a MOSFET (Q1) and a diode (D1) in series. The MOSFET is driven by a PWM signal (PWM) and the diode is connected to ground. The load inductor (L) is connected between the MOSFET and ground.

USB3.1 Type-C Port MUX re-timer ANX7410

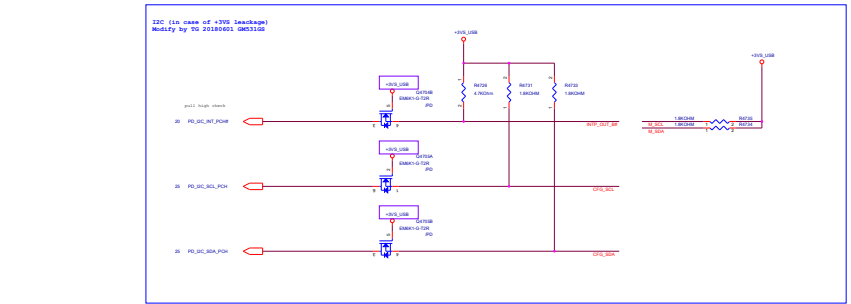
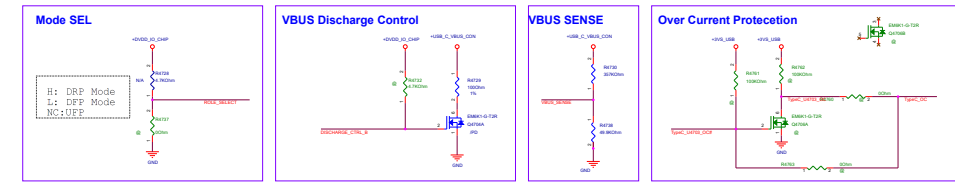
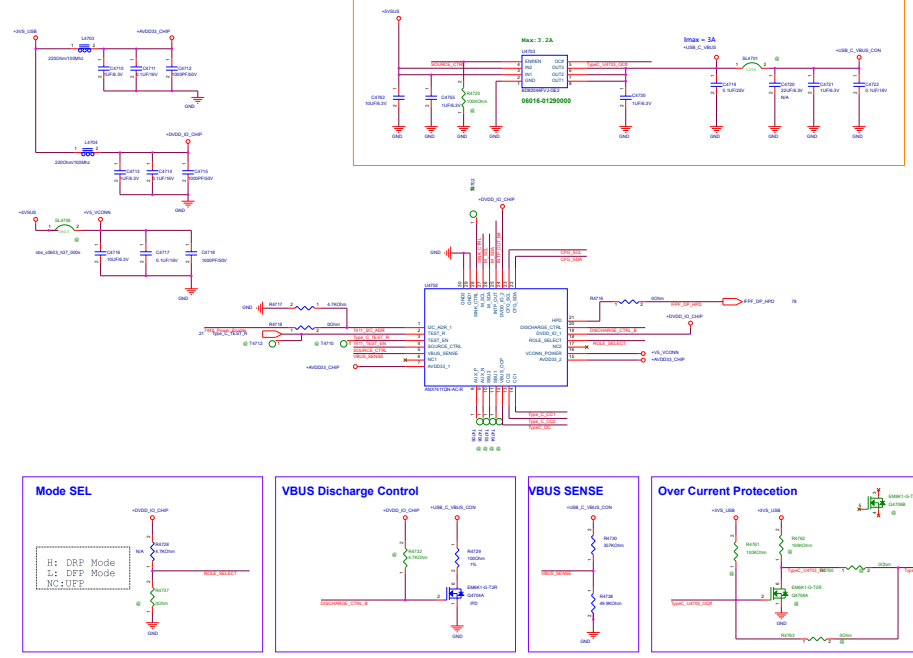


USB2.0 EMI-Protection With ECMF (PCB 1.05mm_10Layer)

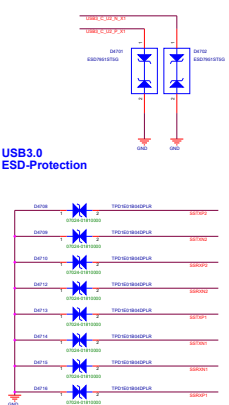


temp_M08_000010 層名順序: TOP/GND/IN1/GND1/IN2/VCC/GND2/IN3/GND3/BOTTOM

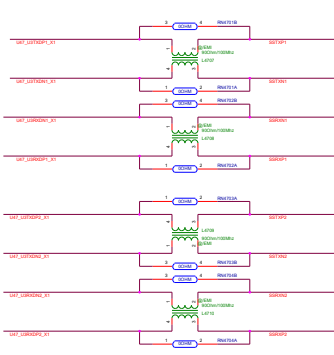
ANX7411



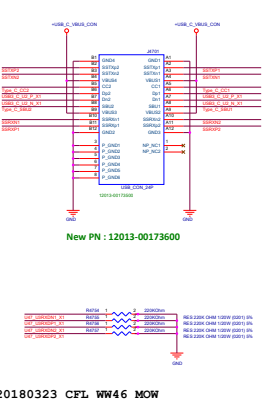
USB2.0 ESD-Protection



USB3.0 EMI-Protection

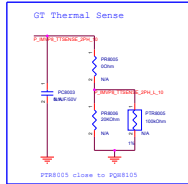


TYPE-C Connector



20180323 CFL WW46 MOW

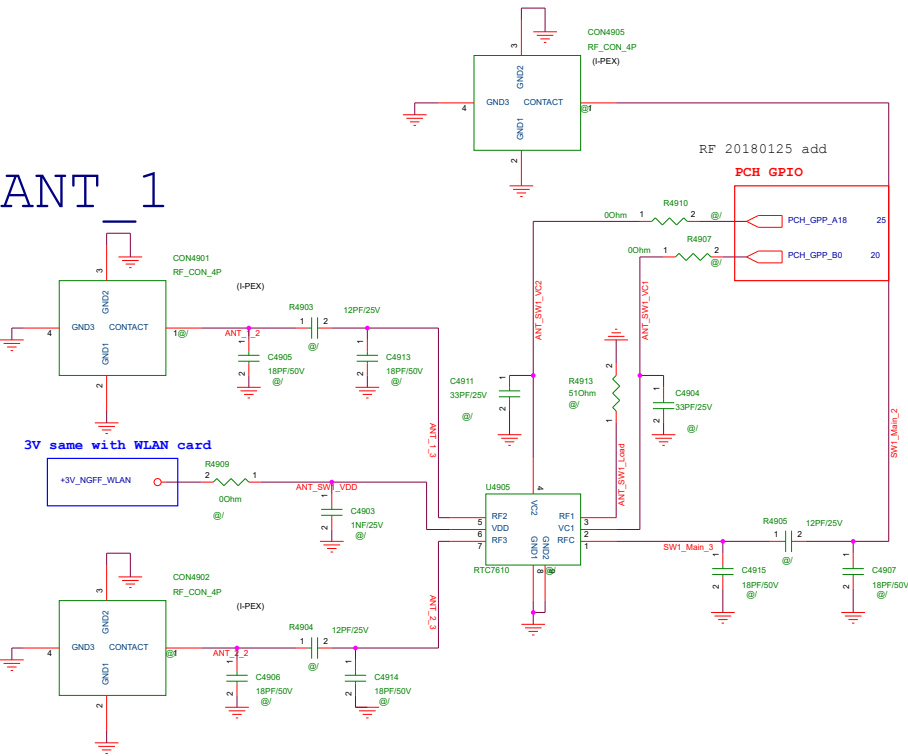
PR8056	N series	G series
65W	13.3Kohm	-
90W	10Kohm	-
120W	10Kohm	40.2Kohm
180W	-	28.7Kohm
230W	-	24.3Kohm



Module_Main

Module_AUX

ANT_1



ANT_2

U5411 RTC7610			
ANT	Port	VC1 GPP_B0	VC2 GPP_A18
50 Ω	RF1	1	0
ANT_1	RF2	X	1
ANT_2	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

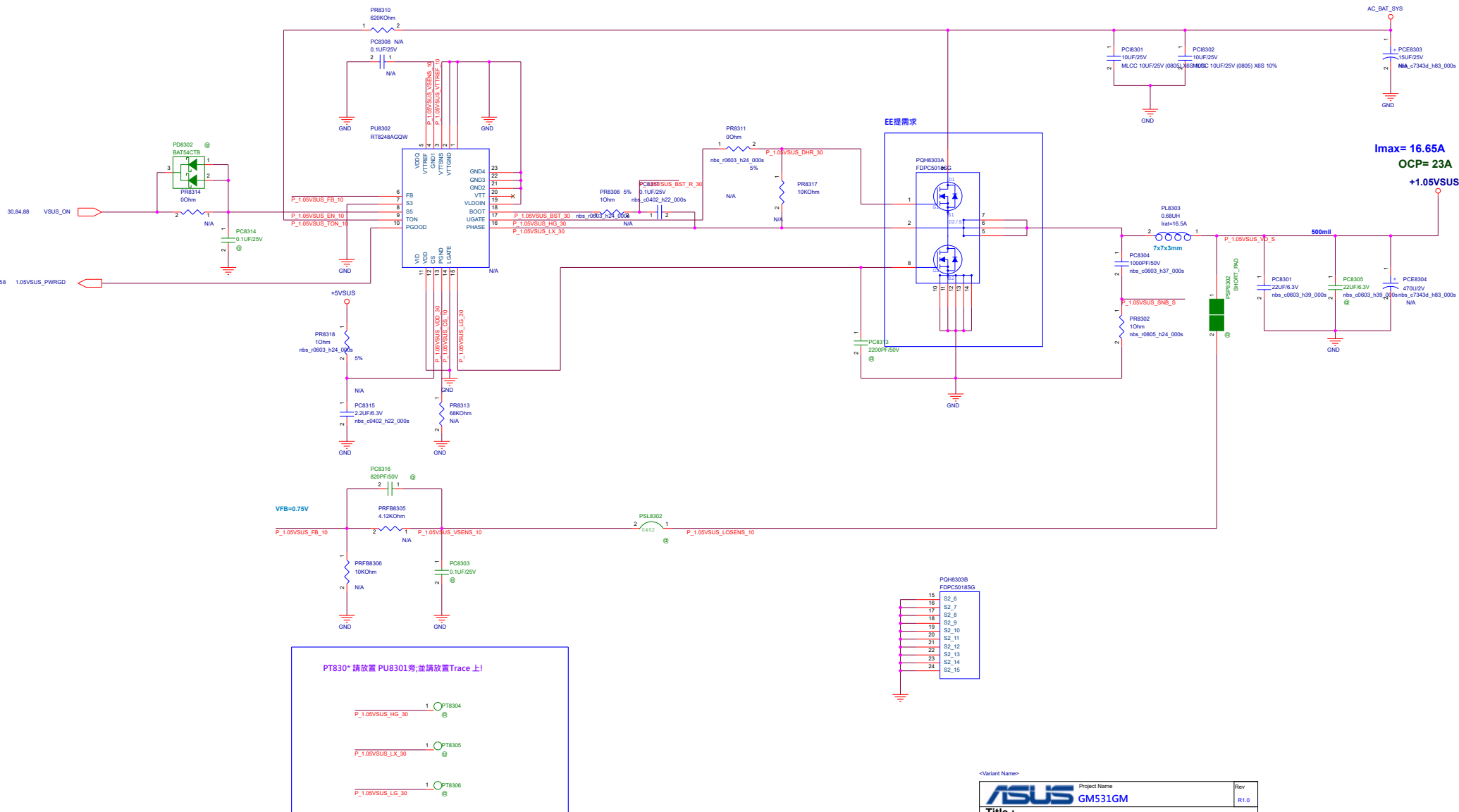
U5412 RTC7610			
ANT	Port	VC1 GPP_B2	VC2 GPP_A19
50 Ω	RF1	1	0
ANT_3	RF2	X	1
ANT_4	RF3	0	0

X: don't care
0: -0.2v~0.3v
1: 1.6v~3.6v

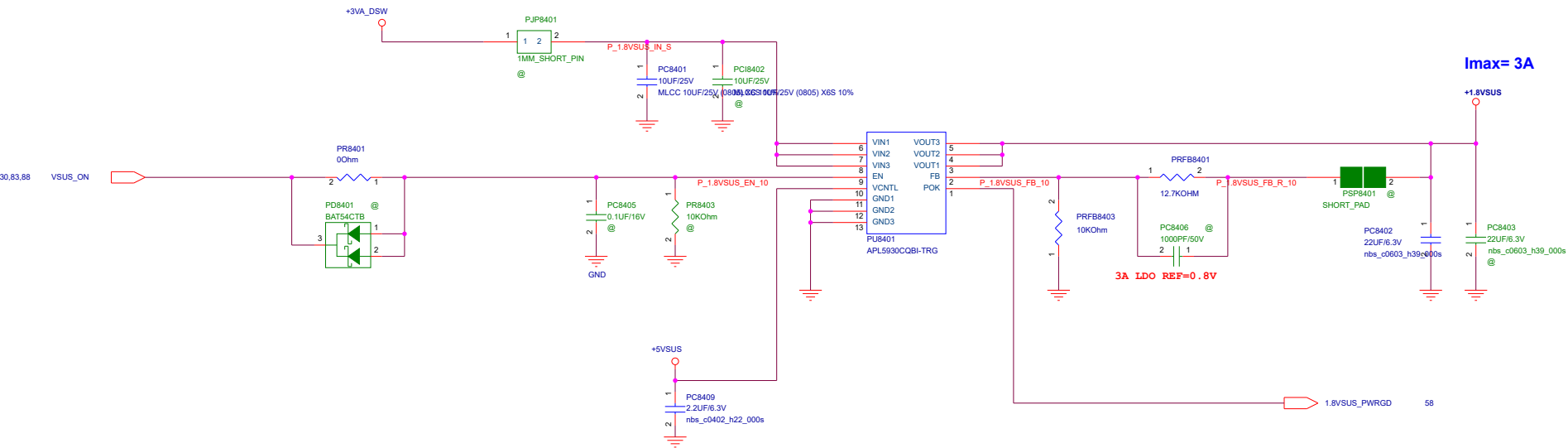
<Core Design>

ASUS		Project Name	Rev
GX531GS			2.0
Title : ANT			
Size	Dept.: ASUSTek COMPUTER	Engineer: EE	
C	Date: Thursday, July 19, 2018	Sheet	49 of 103

+1.05VSUS [For PCH]




+1.8VSUS [For PCH]

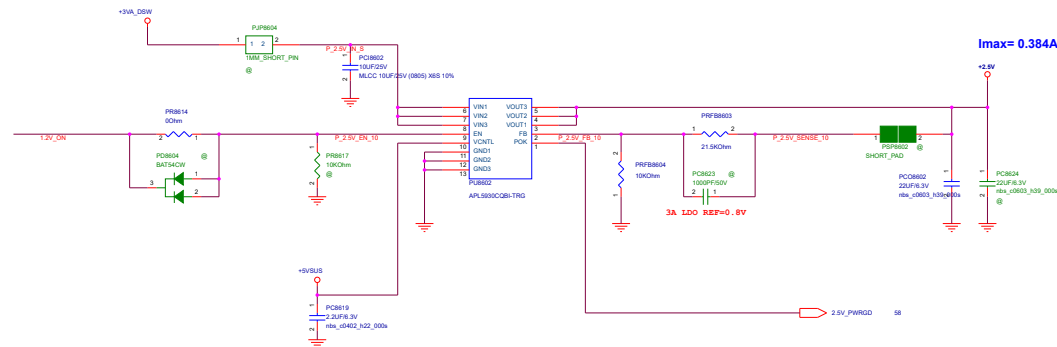
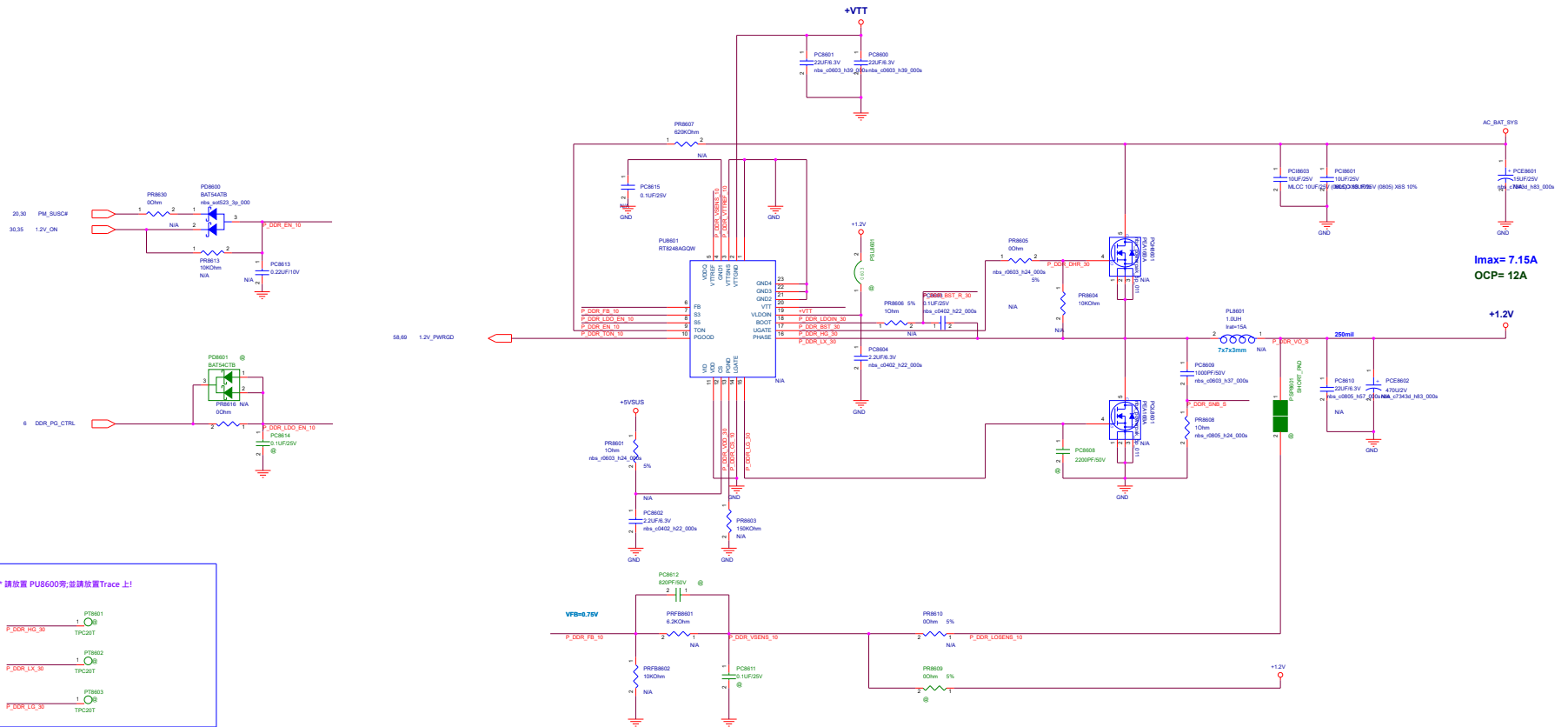


<Variant Name>

ASUS		Project Name	Rev
GM531GM			R1.0
Title : PW_+1.8VSUS			
Size	Dept.:	Engineer: Joe	
Custom	NB Power team		
Date: Thursday, July 19, 2018	Sheet	84	of 103

		Project Name		Rev
		GM531GX		R1.0
Title : Thunderbolt				
Size Custom	Dept.: ASUS Power Team		Engineer:	Joe
Date: Thursday, July 19, 2018			Sheet	85 of 103

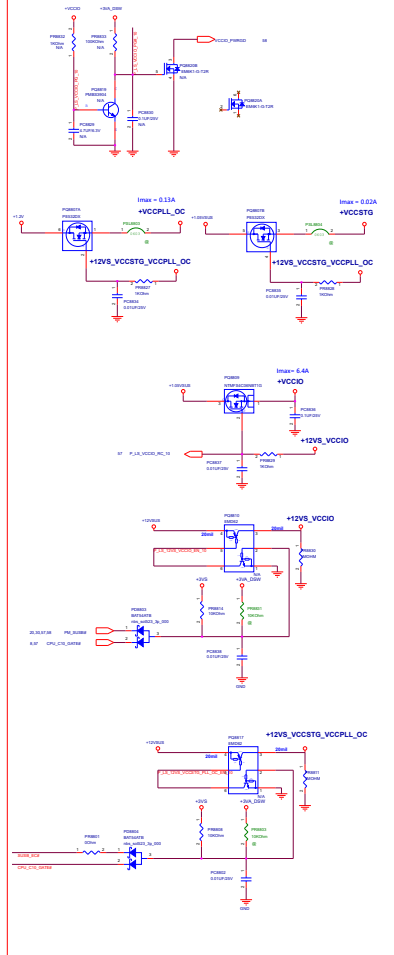
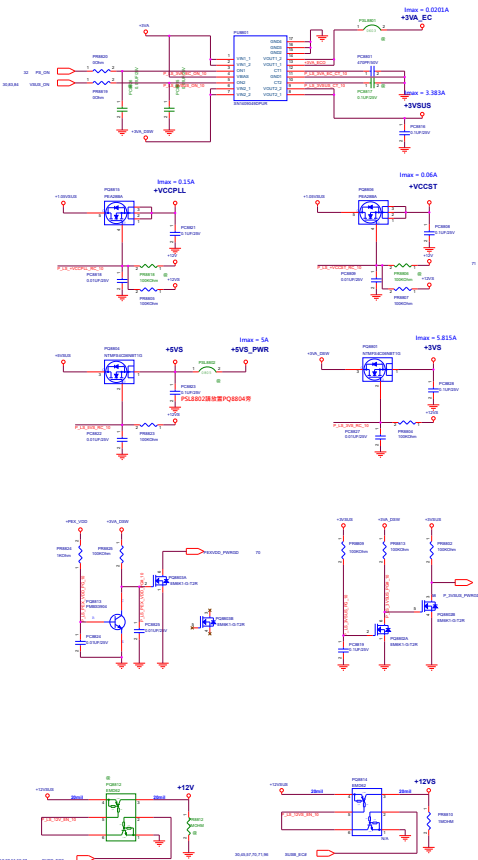
+1.2V / +2.5V [For Memory]





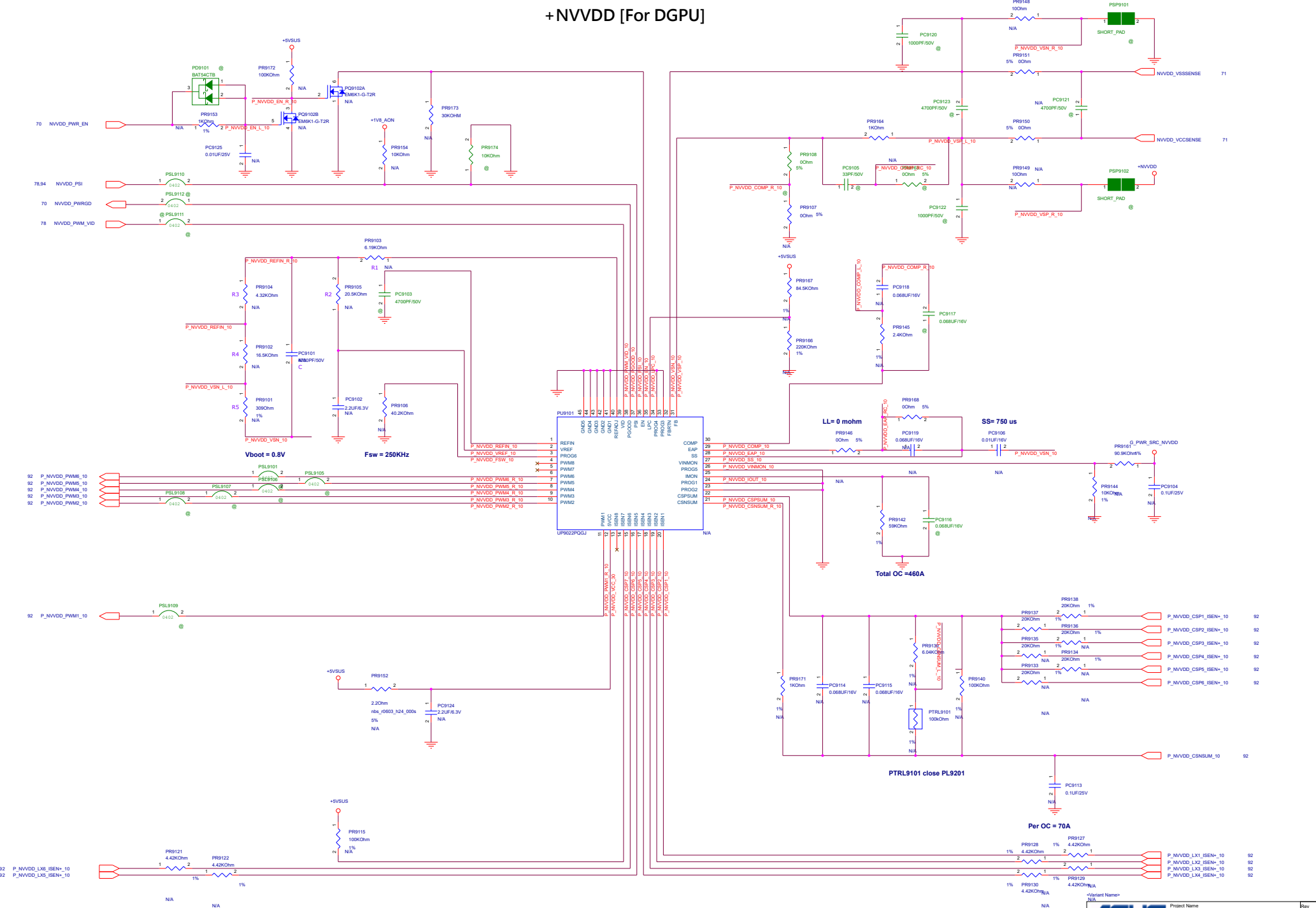
	S0	S1	S3	D03	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	-	1	0	1
1VAD5W_ON	1	-	-	1	0	0	0
2V5US_ON	1	-	-	0	0	0	0
5V5US_ON	1	-	-	1	0	0	1
1.35V_ON	1	-	-	1	0	0	0
SUSC_ECF	1	-	-	0	0	0	0
SUSC_ECF	1	-	-	0	0	0	0






for c10

+NVVDD [For DGPU]

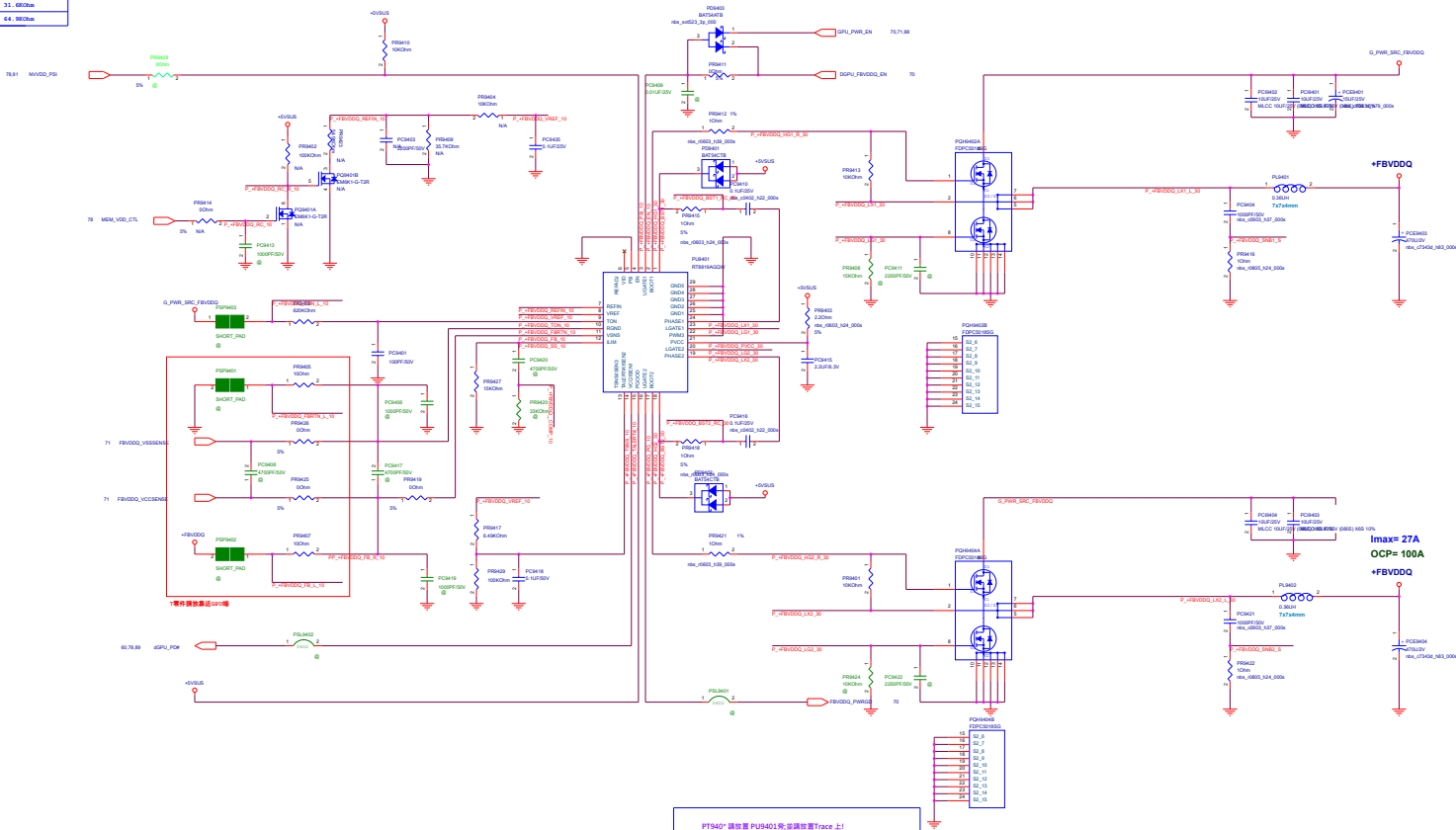


<Variant Name>

		Project Name GX701	Rev R1.0
Title : Thunderbolt			
Size A1	Dept.: ASUS Power Team Engineer: Gaming RD4 EE1		
Date: Thursday, July 19, 2018		Sheet 93	of 103

DVS Setting		
	N17E 8Gb/4Gb	N17E 8Gb Micron
Voltage	1.55V	1.5V
PR3404	100KOhm	100KOhm
PR3409	35.7KOhm	31.6KOhm
PR3423	54.9KOhm	64.9KOhm

+FBVDDQ [For VRAM]



PT940* 請放置 PU9401旁:並請放置Trace 上!



<Variant Name>

Title

<Title>

Size

A

Document Number

<Doc>

Rev

<RevCode>

Date:

Thursday, July 19, 2018

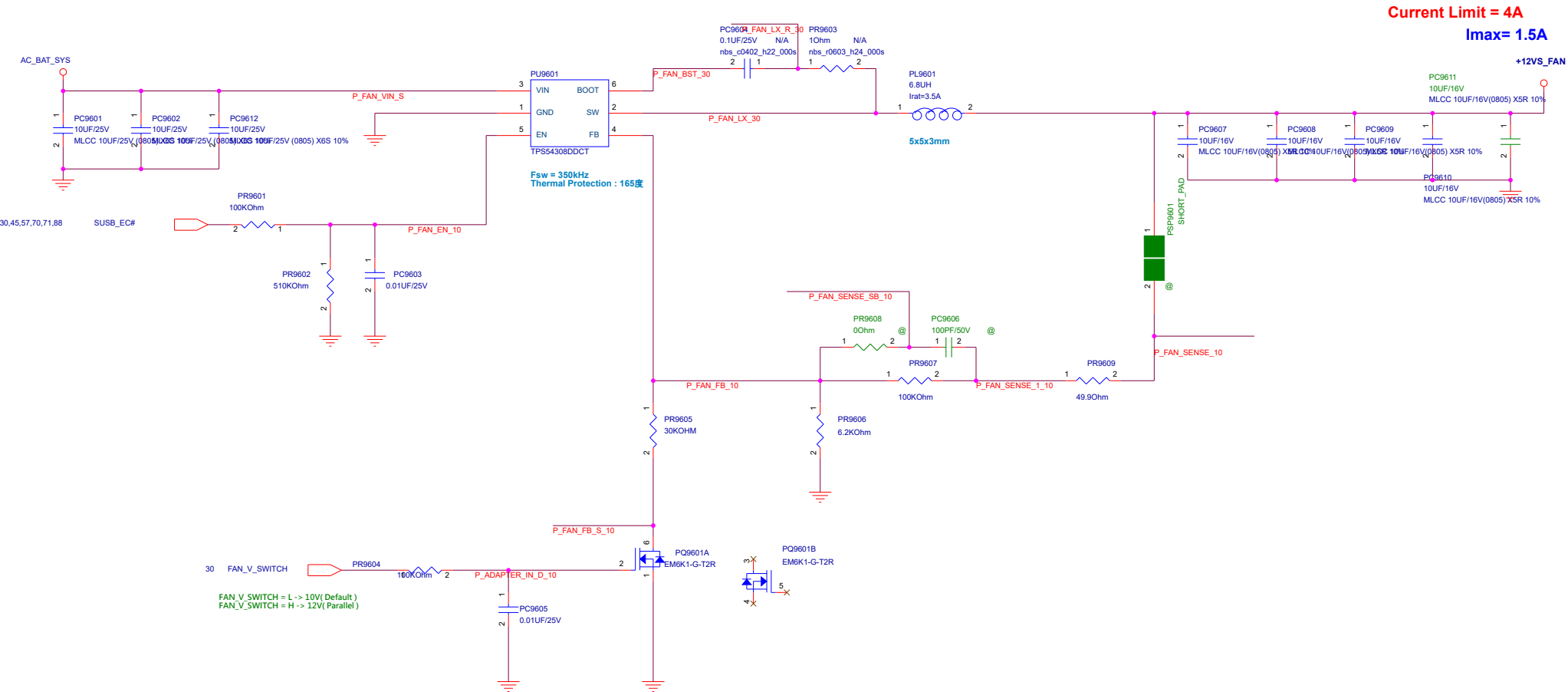
Sheet

95


of

103

+12VS_FAN [For FAN]



<Variant Name>

		Project Name	Rev
GM531GM			R1.0
Title : PW_*12VS_FAN			
Size	Dept.: NS Power team	Engineer:	Joe
B			
Date: Thursday, July 19, 2018		Sheet	96 of 103

GM531GX R1.0 SKU Table

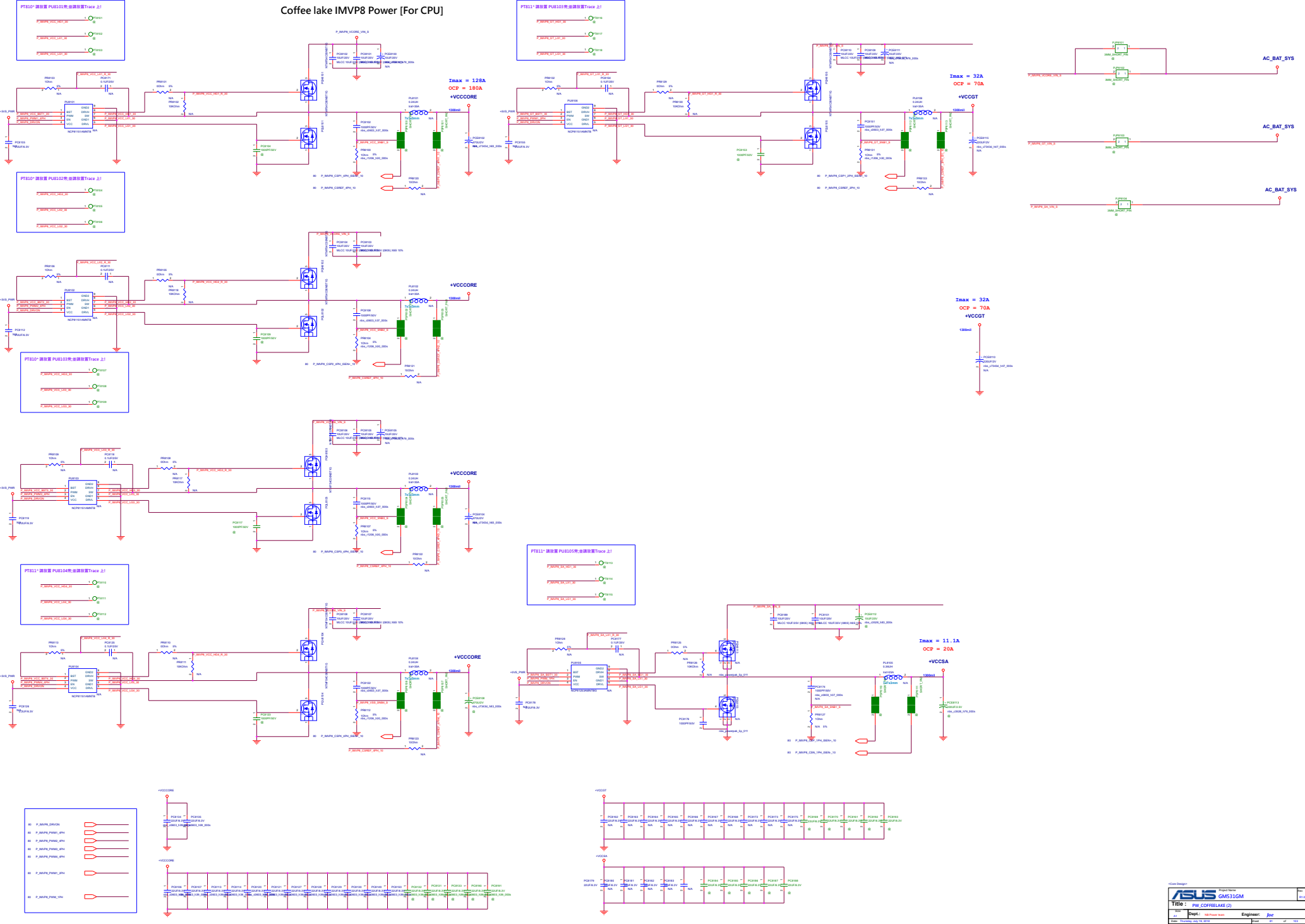
[illegible]


9. Card Reader: AU6435--02G630002400 (Page42)

```
10. USB Charger IC: (Page52) Silago SLG55584AVTR -- 06016-00040000
MAXIM MAX14566AEETA+ -- 06G016196011
```

```
11. USB3.0 Repeater IC: (Page67)
Parade : PS8710B -- 06053-00200000
Maxim : MAX14972CTG+ -- 06053-00030000
```

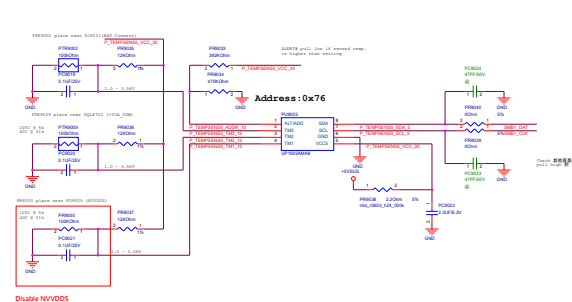
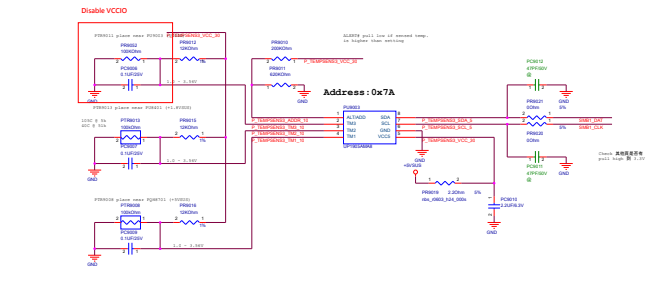
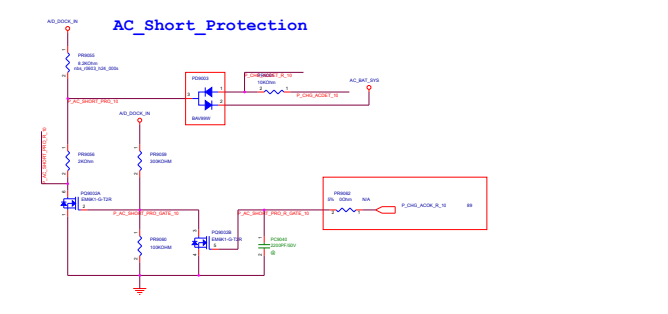
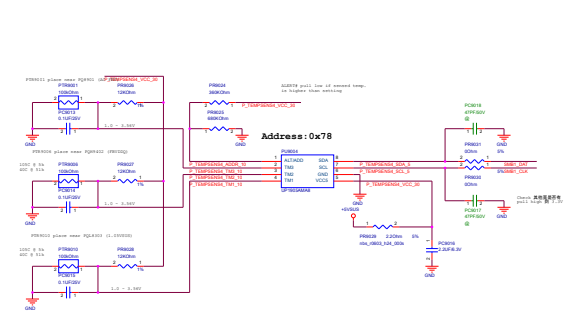
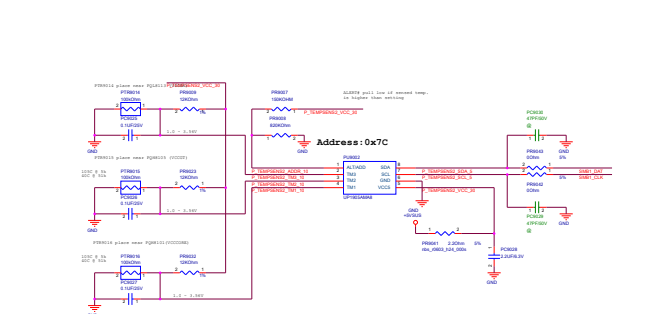
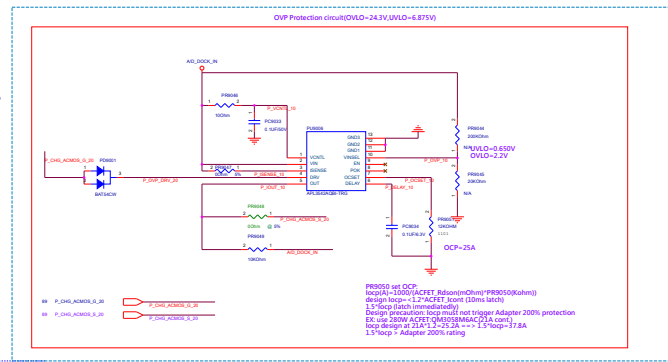
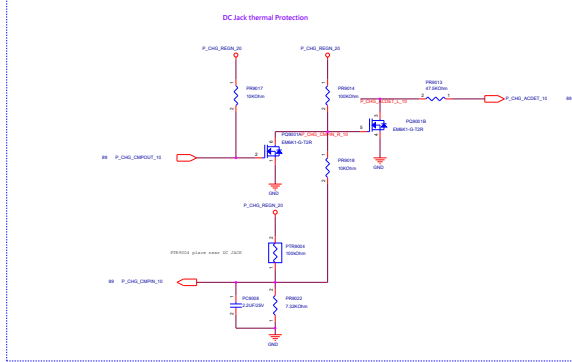
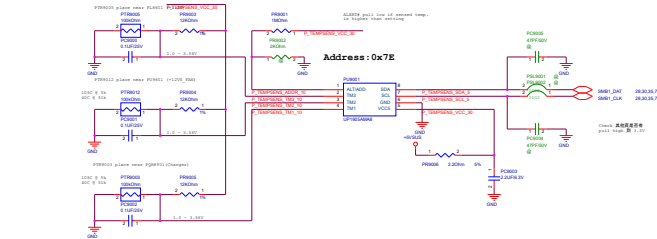




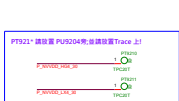
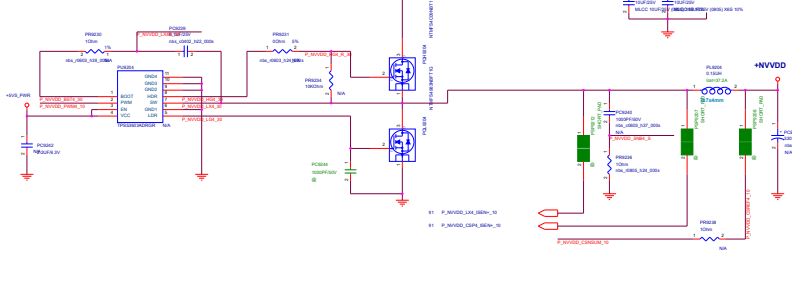
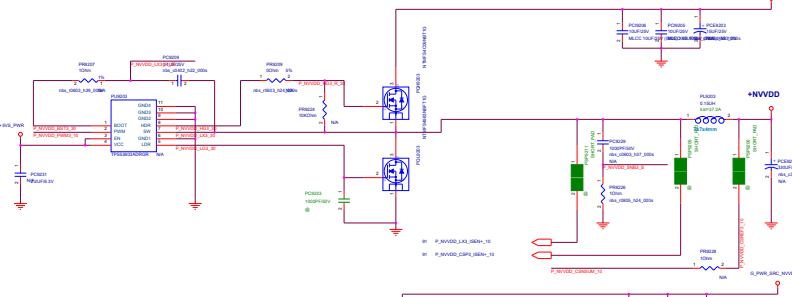
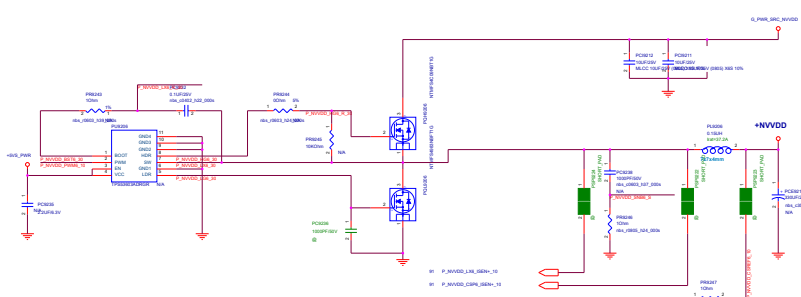
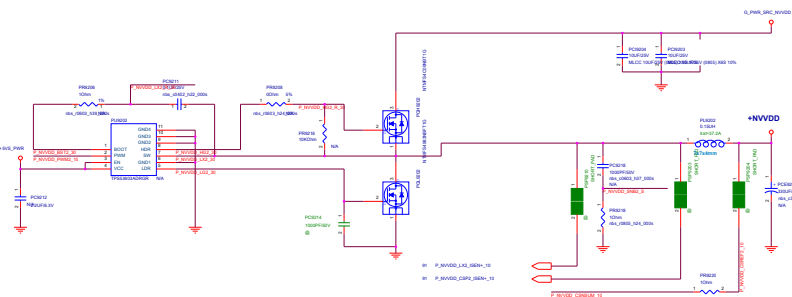
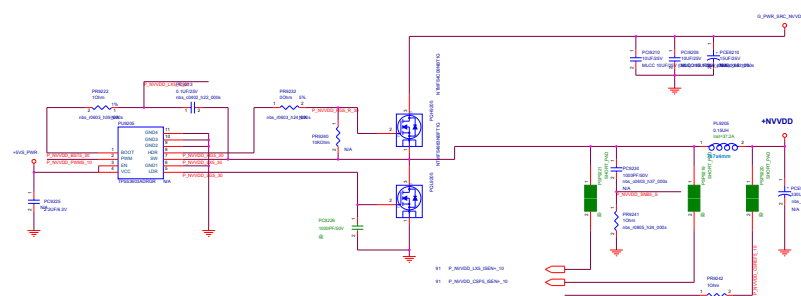
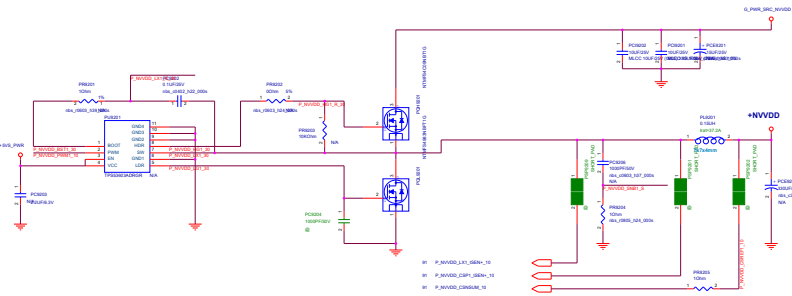
		Project Name GM531GM	Rev R1.0
Title : PW_+VCCIO			
Size A3	Dept.: NB Power team Engineer: <i>Joe</i>		
Date: Thursday, July 19, 2018		Sheet 82	of 103

Address Selection Table									
Address	0x70	0x71	0x72	0x73	0x74	0x75	0x76	0x77	0x78
PSR011	15k	15k	15k	15k	15k	15k	15k	15k	15k
PSR012	15k	15k	15k	15k	15k	15k	15k	15k	15k

Register Address									
Address	0x70	0x71	0x72	0x73	0x74	0x75	0x76	0x77	0x78
PSR011	0	0	0	0	0	0	0	0	0
PSR012	0	0	0	0	0	0	0	0	0



NTC順序有因Layout關係更動過 !!!





Project Name

GM531GX

Rev

R1.0

Title : TBT_TPS65982&Type C

Size

Custom

Dept.: ASUSTeK COMPUTER INC. **Engineer:** Joe

Date: Thursday, July 19, 2018

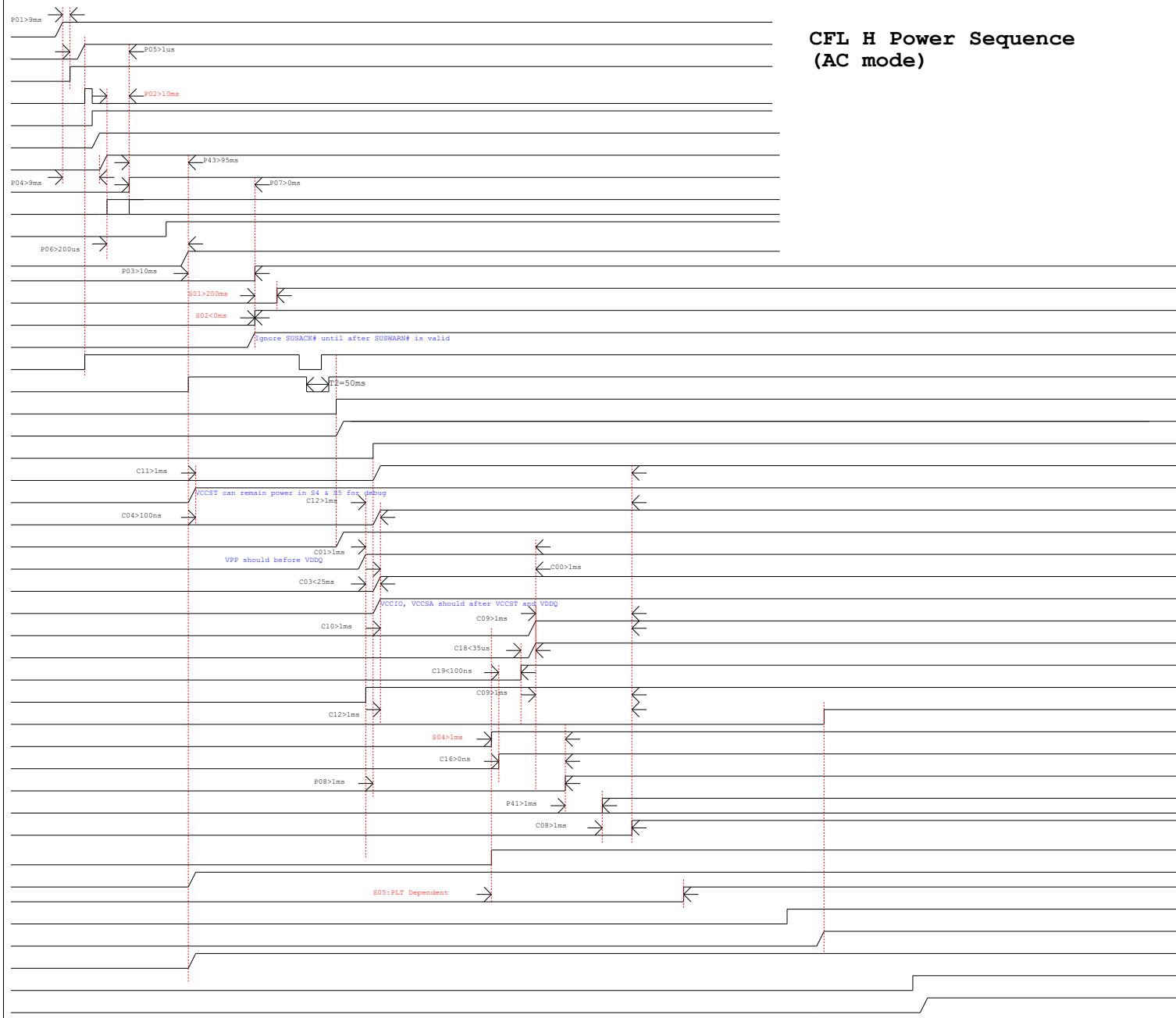
Sheet 97 of 103

C:CPU
P:PCH
S:PLT
Power
Signal

(+RTCBAT)+3VA_RTC
(AC_BAT_SYS)+3VA/+5VA
(+3VA_RTC)RTCRST#(PCH)
(Power)AC_IN_OC#(EC)
(EC)PS_ON(+3VA_EC)
(PS_ON)+3VA_EC(EC)
(3VADSW_ON)+3VA_DSW(3VA_DSW_PWRGD)
(EC)DPWROK_EC(PCH)
(+3VA_DSW)PM_BATLOW#(PCH)
(PCH)PM_SLP_SUS#(EC)
(VSUS_ON)+1.0VSUS_VCCPRIM(1.0VSUS_PWRGD)
(EC)PM_RSMRST#_PCH(PCH)
(PCH)SUSWARN#(EC)
(EC)ME_AC_PRESENT_PCH(PCH)
(EC)PCH_SUSACK#(PCH)
(PWR_Switch)PWR_SW#(EC)
(EC)PM_PWRBTN#(PCH)
(EC)SUSC_EC#(Power)
(SUSC_EC#)+12V/+5V/+3V
(EC)SUSB_EC#(Power)
(SUSB_EC#)+12VS/+5VS/+3VS
(SUSB_EC#)+1.0V_VCCST,VCCPLL
(SUSB_EC#)+VCCIO,(+12VS)+VCCSTG
(1.2V_ON)+2.5V(2.5V_PWRGD)
(1.2V_ON)+VDDQ_CPU(1.2V_PWRGD)
(+12VS)+VCCPLL_OC
(SUSB_EC#)+VCCIO(VCCIO_PWRGD)
(ALL_SYSTEM_PWRGD)+VCCSA(IMVP8_PWRGD)
(DDR_VTT_CTRL)+0.6V
(CPU)DDR_VTT_CTRL(Power)
(Power)1.2V_PWRGD(AND)
(Power)IMVP8_PWRGD
(AND)ALL_SYSTEM_PWRGD(CPU/PCH/EC/Power)
(ALL_SYSTEM_PWRGD)VCCST_PWRGD_CPU(CPU)
(EC)PM_PWROK_PCH(PCH)
(PCH)CLK_PCH_BCLK(CPU)
(PCH)H_CPUPWRGD(CPU)

(CPU)P_SVID_DATA_X2(Power)
(EC)PM_SYSPWROK_PCH(PCH)
(PCH)PLT_RST#(CPU/EC/Device)
(P_IMVP8_DRVON)+VCCCORE(IMVP8_PWRGD)
(CPU)H_THERMTRIP#(PCH)
(PCH)DDR4_DRAMRST#(Memory)

+VCCGT

CFL H Power Sequence
(AC mode)

DC-IN Mode

C:CPU (+RTCBAT)+3VA_RTC
 P:PCH (AC_BAT_SYS)+3VA/+5VA
 S:PLT (+3VA_RTC) RTCRST# (PCH)
 Power (Power) AC_IN_OC# (EC)
 Signal (EC) PS_ON (+3VA_EC)
 (PS_ON)+3VA_EC (EC)
 (3VADSW_ON)+3VA_DSW (3VA_DSW_PWRGD)
 (EC) DPWROK_EC (PCH)
 (+3VA_DSW) PM_BATLOW# (PCH)
 (PCH) PM_SLP_SUS# (EC)
 (VSUS_ON)+1.0VSUS_VCCPRIM (1.0VSUS_PWRGD)
 (EC) PM_RSMRST#_PCH (PCH)
 (PCH) SUSWARN# (EC)
 (EC) ME_AC_PRESENT_PCH (PCH)
 (EC) PCH_SUSACK# (PCH)
 (PWR_Switch) PWR_SW# (EC)
 (EC) PM_PWRBTN# (PCH)
 (EC) SUSC_EC# (Power)
 (SUSC_EC#)+12V/+5V/+3V
 (EC) SUSB_EC# (Power)
 (SUSB_EC#)+12VS/+5VS/+3VS
 (VSUS_ON)+1.0V_VCCST, VCCPLL (VCCST_PWRGD)
 (+VCCIO)+VCCSTG
 (1.2V_ON)+2.5V (2.5V_PWRGD)
 (1.2V_ON)+VDDQ_CPU (1.2V_PWRGD)
 (+12VS)+VCCPLL_OC
 (SUSB_EC#)+VCCIO (VCCIO_PWRGD)
 (ALL_SYSTEM_PWRGD)+VCCSA (IMVP8_PWRGD)
 (DDR_VTT_CTRL)+0.6V
 (CPU) DDR_VTT_CTRL (Power)
 (Power) 1.2V_PWRGD (AND)
 (Power) IMVP8_PWRGD
 (AND) ALL_SYSTEM_PWRGD (CPU/PCH/EC/Power)
 (ALL_SYSTEM_PWRGD) VCCST_PWRGD_CPU (CPU)
 (EC) PM_PWROK_PCH (PCH)
 (PCH) CLK_PCH_BCLK (CPU)
 (PCH) H_CPU_PWRGD (CPU)
 (ALL_SYSTEM_PWRGD) P_IMVP8_EN_10 (Power)
 (CPU) P_SVID_DATA_X2 (Power)
 (EC) PM_SYSPWROK_PCH (PCH)
 (PCH) PLT_RST# (CPU/EC/Device)
 (P_IMVP8_DRVON)+VCCCORE (IMVP8_PWRGD)
 (CPU) H_THERMTRIP# (PCH)
 (PCH) DDR4_DRAMRST# (Memory)

+VCCGT

CFL H Power Sequence (DC mode)

